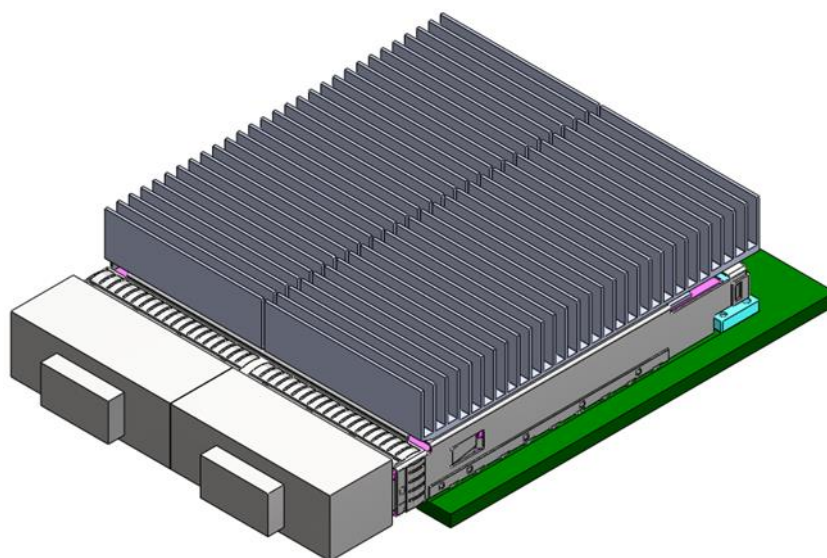




CFP8 Hardware Specification

Revision 1.0

17-March, 2017



Description:

This CFP Multi-Source Agreement (MSA) defines the CFP8 form factor of an optical transceiver to support 400 Gb/s interfaces for Ethernet, Telecommunication and other applications. The members of the CFP MSA have authored this document to provide an industry standard form factor for new and emerging high speed communications interfaces. Specifications provided in this document are a “delta” to: the CFP MSA Hardware Specification Rev.1.4, June 7, 2010 [1]; the CFP MSA CFP2 Hardware Specification Rev.1.0, July 31, 2013 [2]; and the CFP MSA CFP4 Hardware Specification Rev. 1.1, March 20, 2015 [3].

CFP MSA Member Contacts

CFP8 Hardware Technical Editor	David Lewis	David.Lewis@lumentum.com
--------------------------------	-------------	--------------------------

Finisar Corporation	Chris Cole	chris.cole@finisar.com
Oclaro, Inc.	Kiyo Hiramoto	kiyohisa.hiramoto@oclaro.com
Sumitomo Electric Industries, Ltd./ Sumitomo Electric Device Innovations, Inc./Sumitomo Electric Device Innovations U.S.A., Inc.	Eddie Tsumura	tsumura-eiji@sei.co.jp
Foxconn Interconnect Technology Limited (On behalf of itself and Foxconn Optical Interconnect Technologies, Inc.)	John Petrilla	john.petrilla@foit-foxconn.com
Fujitsu Optical Components	Yasunori Nagakubo	nagakubo.yasuno@jp.fujitsu.com
Lumentum Operations LLC	David Lewis	David.Lewis@lumentum.com
NeoPhotonics Corporation	Winston Way	Winston.way@neophotonics.com

REVISION HISTORY

Draft	Date	Revised Items
0.1	7/14/2016	Initial draft, based on CFP8 Baseline Design
0.2	8/1/2016	Corrections identified by MSA members
0.3	9/30/2016	Changes from Comment_Log_CFP8_HW_V0p2_ByCls.xlsx
0.4	11/28/2016	Changes from Comment_Log_CFP8_HW_V0p3_MasterList.xlsx
0.5	12/12/2016	Minor corrections. Low power mode to 2W. Added figures 5-3, 5-6 and 5-7
0.9	1/20/2017	First public draft. Resolved comments from OEM system reviewers.
1.0	3/17/2017	First public release.

CONTENTS

1	GENERAL	10
1.1	SCOPE.....	10
1.2	CFP8 FUNCTIONAL BLOCK DIAGRAM	11
1.3	FUNCTIONAL DESCRIPTION.....	11
1.3.1	<i>Hot Pluggable</i>	11
2	CFP8 HARDWARE SIGNALING PINS	12
2.1	HARDWARE CONTROL PINS	12
2.2	HARDWARE CONTROL PINS: FUNCTIONAL DESCRIPTION	12
2.2.1	<i>Programmable Control (PRG_CNTL)</i>	12
2.2.2	<i>TX Disable Pin</i>	13
2.3	HARDWARE ALARM PINS	13
2.4	HARDWARE ALARM PINS: FUNCTIONAL DESCRIPTION.....	14
2.4.1	<i>Programmable Alarm (PRG_ALRM)</i>	14
2.4.2	<i>Receiver Loss of Signal Pin</i>	14
2.5	MANAGEMENT INTERFACE PINS	15
2.5.1	<i>Baseline MDIO Arrangement (Required)</i>	15
2.5.2	<i>Optional MDIO Arrangement</i>	16
2.6	CFP8 MANAGEMENT INTERFACE HARDWARE DESCRIPTION	16
2.7	HARDWARE SIGNALING PIN ELECTRICAL SPECIFICATIONS	16
2.7.1	<i>Control & Alarm Pins: 3.3V LVCMOS Electrical Characteristics</i>	16
2.7.2	<i>MDIO Interface Pins: 1.2V LVCMOS Electrical Characteristics</i>	17
2.8	HARDWARE SIGNALING PIN TIMING REQUIREMENTS.....	18
2.8.1	<i>Optional MOD_SELn Timing Requirements</i>	18
3	MODULE MANAGEMENT INTERFACE DESCRIPTION	19
3.1	BASELINE: DEDICATED MDIO BUS PER CFP8 MODULE	19

3.2	OPTIONAL: MDIO BUS SHARED BETWEEN MULTIPLE CFP8 MODULES	19
4	PERFORMANCE SPECIFICATIONS	21
4.1	OPERATING ENVIRONMENT	21
4.2	POWER SUPPLIES AND POWER DISSIPATION	21
4.2.1	<i>Voltage power supply and power dissipation.....</i>	<i>21</i>
4.2.2	<i>Inrush current.....</i>	<i>21</i>
4.2.3	<i>Turn-off current</i>	<i>21</i>
4.2.4	<i>Power Supply Noise Susceptibility.....</i>	<i>21</i>
4.2.5	<i>Grounding.....</i>	<i>23</i>
4.3	OPTICAL CHARACTERISTICS.....	23
4.3.1	<i>Optical Specifications.....</i>	<i>23</i>
4.4	HIGH SPEED ELECTRICAL CHARACTERISTICS	23
4.4.1	<i>25.78125 Gb/s NRZ Transmitter Data (and Clock).....</i>	<i>24</i>
4.4.2	<i>25.78125 Gb/s NRZ Receiver Data (and Clock).....</i>	<i>24</i>
4.4.3	<i>26.5625 Gb/s NRZ Transmitter Data (and Clock).....</i>	<i>24</i>
4.4.4	<i>26.5625 Gb/s NRZ Receiver Data (and Clock).....</i>	<i>24</i>
4.4.5	<i>26.5625 GBd PAM-4 Transmitter Data (and Clock)</i>	<i>24</i>
4.4.6	<i>26.5625 GBd PAM-4 Receiver Data (and Clock).....</i>	<i>24</i>
4.4.7	<i>Loopback (Optional).....</i>	<i>25</i>
4.4.8	<i>Reference Clock (Optional).....</i>	<i>25</i>
4.4.9	<i>Transmitter Monitor Clock (Optional)</i>	<i>27</i>
4.4.10	<i>Receiver Monitor Clock (Optional)</i>	<i>27</i>
4.4.11	<i>Monitor Clock (Optional).....</i>	<i>27</i>
5	MECHANICAL SPECIFICATIONS	30
5.1	MECHANICAL OVERVIEW.....	30
5.2	ELECTRICAL CONNECTOR.....	32

5.2.1	Module Plug Connector.....	32
5.2.2	Host Connector	33
5.2.3	Connector Pin Contact Mating	34
5.3	CFP8 MODULE DIMENSIONS	34
5.3.1	CFP8 Mechanical Surface Characteristics	36
5.3.2	CFP8 Insertion & Extraction.....	37
5.4	HOST SYSTEM DIMENSIONS.....	38
5.5	RIDING HEAT SINK	38
5.6	OPTICAL CONNECTORS	39
5.6.1	Optional Optical LC Connector Position for Telecom Applications.....	40
5.7	ELECTRICAL CONNECTORS.....	40
5.8	PIN ASSIGNMENT	41
5.9	CFP8 LABELING.....	48
6	REGULATORY COMPLIANCE	49

TABLE LIST

Table 2-1: Hardware Control Pins.....	12
Table 2-2: Hardware Alarm Pins.....	14
Table 2-3: Management Interface Pins (MDIO)	15
Table 2-4: Optional MOD_SEL _n Timing Parameters	18
Table 4-1: Voltage Power Supply	22
Table 4-2: Optional Reference Clock Characteristics.....	26
Table 4-3: Optional Monitor Clock Characteristics	27
Table 4-4: CFP8 Module Clocking Signals.....	28
Table 5-1: CFP8 Mechanical Characteristics	36
Table 5-2: CFP8 Module Insertion, Extraction Forces.....	37
Table 5-3: Optical Connectors	39
Table 5-4: CFP8 Host Connector Assembly	40
Table 5-5: CFP8 Pin Map	42
Table 5-6: CFP8 Top Row Pin Descriptions.....	43
Table 5-7: CFP8 Bottom Row Pin Descriptions	45
Table 5-8: CFP8 Bail Latch Color Coding	48

FIGURE LIST

Figure 1-1: CFP8 Functional Block Diagram.....	11
Figure 2-1: Reference +3.3V LVCMOS Output Termination	16
Figure 2-2: Reference 3.3V LVCMOS Input Termination	17
Figure 2-3: Reference MDIO Interface Termination	17
Figure 2-4: Optional MOD_SEL _n Timing Diagram	18
Figure 3-1 PHYADR Setup Sequence for Optional Shared MDIO bus.....	20
Figure 4-1: High Speed I/O for Data and Clocks.....	23
Figure 4-2: CFP8 Module Optional Loopback Orientation.....	25
Figure 4-3: Example of Clocking for 16 x 25 Gb/s CFP8 Applications.....	29
Figure 4-4: Example of Clocking for 8 x 50 Gb/s PAM-4 CFP8 Applications	29
Figure 5-1: CFP8 Module & CFP8 Module Mated in Single and Dual Port Systems	30
Figure 5-2: Host Cage System and Mounting Method Overview.....	31
Figure 5-3: CFP8 Module Plug Connector Assembly	32
Figure 5-4: CFP8 Single & Double Port Host Connector Cover Assemblies	33
Figure 5-5: CFP8 Host Connector Assembly	33
Figure 5-6: CFP8 Pin Map Connector Engagement.....	34
Figure 5-7: CFP8 Module Dimension Overview	35
Figure 5-8: Riding Heat Sink.....	38
Figure 5-9: Host Cage Top Surface Opening.....	39
Figure 5-10: CFP8 Optical Connector Position	40
Figure 5-11: CFP8 Connector Pin Map Orientation.....	41
Figure 5-12 CFP8 Pin Map for Multiple Configurations	47
Figure 5-13: CFP8 Module Label Recess	48

REFERENCE DOCUMENTS

- [1] CFP MSA Hardware Specification, Revision 1.4, June 7, 2010. <http://www.cfp-msa.org/Documents/CFP-MSA-HW-Spec-rev1-40.pdf>
- [2] CFP MSA CFP2 Hardware Specification, Revision 1.0, July 31, 2013. http://www.cfp-msa.org/Documents/CFP2_HW-Spec-rev1.0.pdf
- [3] CFP MSA CFP4 Hardware Specification, Revision 1.1, March 18, 2015. http://www.cfp-msa.org/Documents/CFP-MSA_CFP4_HW-Spec-rev1.1.pdf
- [4] CFP MSA Management Interface Specification, Version 2.4, June 8, 2015. http://www.cfp-msa.org/Documents/CFP_MSA_MIS_V2p4r06b.pdf (to be updated)
- [5] IEEE P802.3bs, 400 Gb/s Ethernet Task Force, <http://ieee802.org/3/bs/index.html>
- [6] IEEE Std. 802.3™-2015, Annexes 83A, 83B, 83E, 86A. <http://standards.ieee.org/about/get/802/802.3.html>
- [7] IEEE Std. 802.3™-2015, Cl. 45, Management Data Input/Output (MDIO) Interface. <http://standards.ieee.org/about/get/802/802.3.html>
- [8] ITU-T Recommendation G.709 (2012) *Interfaces for the Optical Transport Network (OTN)*. <http://www.itu.int/rec/T-REC-G/en>
- [9] ITU-T Recommendation G.707 (2007) *Network node interface for the synchronous digital hierarchy (SDH)*. <http://www.itu.int/rec/T-REC-G/en>
- [10] OIF-CEI-3.1, Common Electrical I/O (CEI) – Electrical and Jitter Interoperability Agreements for 6G+ bps, 11G+ bps and 25G+ bps I/O, February 18, 2014. http://www.oiforum.com/public/documents/OIF_CEI_03.1.pdf
- [11] SNIA SFF TA TWG INF-8077i 10 Gigabit Small Form Factor Pluggable Module. <http://www.snia.org/sff/specifications>
- [12] SNIA SFF TA TWG SFF-8431 SFP+ 10 Gb/s and Low Speed Electrical Interface. <http://www.snia.org/sff/specifications>

1 GENERAL

1.1 SCOPE

This hardware specification defines the CFP8 form factor for a 400 Gb/s optical transceiver used for Ethernet and other applications. Specifications provided in this document are a “delta” to the CFP MSA Hardware Specification [1]; the CFP2 Hardware Specification [2]; and the CFP4 Hardware Specification [3].

The CFP8 electrical interface supports up to 16 differential lanes in each direction with nominal signaling rates of 25.78125 or 26.5625 GBd per lane, and either NRZ or PAM-4 signaling. Documentation of the electrical signaling specifications are provided in [6], [10] and in the working documents of ongoing IEEE and OIF projects [5]. The CFP8 module may be used to support single-mode or multi-mode optical fiber media.

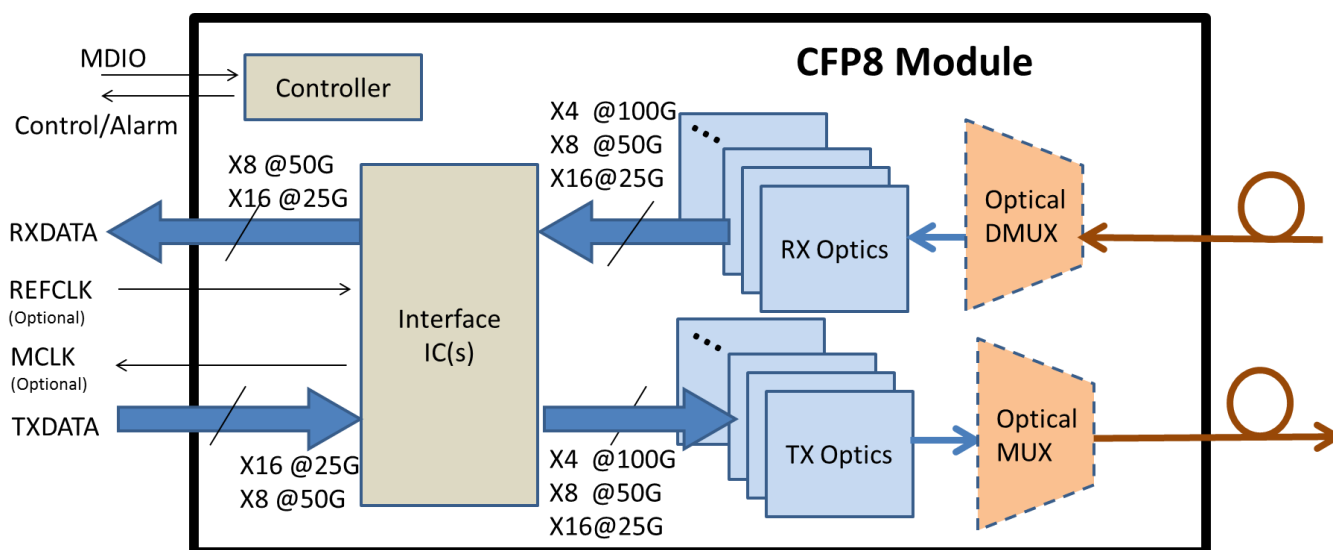
CFP8 modules and the host system are hot-pluggable. The module or the host system shall not be damaged by insertion or removal of the module.

CFP MSA is an acronym for 100G¹ Form Factor Pluggable Multi-Source Agreement. The CFP8 supports eight times and four times the bandwidth-density of CFP and CFP2 form factors, respectively.

¹ C = 100 in Roman numerals (Centum).

1.2 CFP8 FUNCTIONAL BLOCK DIAGRAM

Figure 1-1: CFP8 Functional Block Diagram



1.3 FUNCTIONAL DESCRIPTION

The CFP8 module is a hot pluggable form factor designed for optical networking applications. The module size has been chosen to accommodate a wide range of power dissipations and applications. The module electrical interface has been generically specified to allow for supplier-specific customization around various 16 x 25 Gb/s and 8 x 50 Gb/s interfaces.

1.3.1 Hot Pluggable

A CFP8 module is defined to be hot pluggable. Hot Pluggable is defined as permitting module plugging and unplugging with Vcc applied, with no module damage and predictable module behavior as per the State Transition Diagram. As shown in Figure 5-6: Pin Map Connector Engagement, the Module Absent (MOD_ABS) pin and Module Low Power (MOD_LOPWR) pin are physically guaranteed to be one of the last pins to mate.

2 CFP8 HARDWARE SIGNALING PINS

The control and status reporting functions between a host and a CFP8 module use non-data control and status reporting pins on the 124-pin connector. The control and status reporting pins work together with the MDIO interface to form a complete HOST-CFP8 management interface. The status reporting pins provide status reporting. There are three (3) Hardware Control pins, two (2) Hardware Alarm pins, and four (4) pins dedicated to the MDIO interface. Specification of the CFP8 hardware signaling pins are given in Ref.[1] with the following changes listed in this document.

2.1 HARDWARE CONTROL PINS

The CFP8 Module supports real-time control functions via hardware pins, listed in Table 2-1. Specifications of the CFP8 hardware control pins are given in Ref. [1], with the changes listed below.

Table 2-1: Hardware Control Pins

Pin #	Symbol	Description	I/O	Logic	“H”	“L”	Pull-up /down
96	TX_DIS (PRG_CNTL1)	Transmitter Disable (Optionally configurable as Programmable Control after Reset ¹)	I	3.3V LVCMOS	Disable ²	Enable ²	Pull – Up ³
94	MOD_LOPWR	Module Low Power Mode	I	3.3V LVCMOS	Low Power	Enable	Pull – Up ³
88	MOD_RSTn	Module Reset, Active Low (invert)	I	3.3V LVCMOS	Enable	Reset	Pull – Down ⁴

¹ When Programmable Control is configured, MSA Default is TX_DIS.

² Per CFP MSA Management Interface Specification [4] when PRG_CNTL1 is configured for this pin.

³ Pull-Up resistor (4.7 kOhm to 10 kOhm) is located within the CFP8 module

⁴ Pull-Down resistor (4.7 kOhm to 10 kOhm) is located within the CFP8 module

2.2 HARDWARE CONTROL PINS: FUNCTIONAL DESCRIPTION

2.2.1 *Programmable Control (PRG_CNTL)*

This control pin allows for the system to program certain controls via a hardware pin. TX Disable Pin (TX_DIS) is optionally configurable as Programmable Control 1 Pin after Reset. When Programmable Control 1 is configured, the default setting for Control 1 is control of the TX_DIS.

CFP MSA CFP8 Hardware Specification, Revision 1.0

2.2.1.1 Programmable Control 1 Pin (PRG_CNTL1)

Programmable Control 1 Pin is an input pin from the Host, operating with programmable logic. This pin is pulled up in the CFP8 module. It can be re-programmed over MDIO registers to another MDIO control register while the module is in any steady state except Reset. The CFP MSA specifies that the default function be TX Disable (TX_DIS) with active-high logic. If the other function besides TX_DIS is configured for this pin, there is no way to assert TX disable via a hardware pin.

2.2.1.2 Programmable Control 2 Pin

Not supported in CFP8 module

2.2.1.3 Programmable Control 3 Pin

Not supported in CFP8 module

2.2.1.4 Hardware Interlock

Not supported in CFP8 module

2.2.2 TX Disable Pin

TX Disable Pin (TX_DIS) is an input pin from the Host, operating with active-high logic. This pin is pulled up in the CFP8. When TX_DIS is asserted, all of the optical outputs inside a CFP8 module shall be turned off. When this pin is de-asserted, transmitters in a CFP8 module shall be turned on according to a predefined TX turn-on process which is defined by the state diagram shown in the “CFP MSA Management Interface Specification”. A maximum time is defined for the transmitter turn-on process. This time is vendor and/or technology specific and the value is stored in a MDIO register.

This pin can be optionally configured as Programmable Control 1 Pin after Reset. One MDIO register which defines if the module supports this optional configuration or not, is prepared in the NVR region.

Please refer to Ref. [4] for more details.

2.3 HARDWARE ALARM PINS

The CFP8 Module supports alarm hardware pins as listed in Table 2-2. Specifications of the CFP8 hardware alarm pins are given in Ref. [1].

Table 2-2: Hardware Alarm Pins

Pin #	Symbol	Description	I/O	Logic	“H”	“L”	Pull-up /down
95	RX_LOS (PRG_ALARM1)	Receiver Loss of Signal (Optionally configurable as Programmable Alarm after Reset ¹)	O	3.3V LVCMOS	Loss of Signal ²	OK ²	
93	MOD_ABS	Module Absent	O	3.3V LVCMOS	Absent	Present	Pull Down ³

¹ When Programmable Alarm is configured, MSA Default is RX_LOS.

² Active High per CFP MSA MIS Ref. [4] when PRG_ALARM1 is configured for this pin.

³ Pull-Down resistor (<100 Ohm) is located within the CFP8 module. Pull-up should be located on the host.

2.4 HARDWARE ALARM PINS: FUNCTIONAL DESCRIPTION

2.4.1 Programmable Alarm (PRG_ALARM)

This alarm pin allows for the system to program module supported alarms to a hardware pin. The intention is to allow for maximum design and debug flexibility.

2.4.1.1 Programmable Alarm 1 Pin

Programmable Alarm 1 Pin (PRG_ALARM1) is an output pin to the Host, operating with programmable logic. This pin can be re-programmed over MDIO registers to another MDIO alarm register while the module is in any steady state except Reset. CFP-MSA specifies the default function to be Receiver Loss of Signal (RX_LOS) indicator with active-high logic.

2.4.1.2 Programmable Alarm 2 Pin

Not supported in CFP8 module

2.4.1.3 Programmable Alarm 3 Pin

Not supported in CFP8 module

2.4.2 Receiver Loss of Signal Pin

The Receiver Loss of Signal Pin (RX_LOS) is an output pin to the Host, operating with active-high logic. When asserted, it indicates received optical power in the CFP8 module is lower than the expected value. The optical power at which RX_LOS is asserted may be specified by other governing documents and the

CFP8 module vendor as the alarm threshold level is application specific. The RX_LOS is the logic OR of the LOS signals from all the input receiving channels in a CFP8 module.

This pin can be optionally configured as Programmable Alarm 1 Pin after Reset. One MDIO register which defines if the module supports this optional configuration or not is prepared in NVR region.

Please refer to Ref. [4] for more details.

2.5 MANAGEMENT INTERFACE PINS

The CFP8 Module supports alarm, control and monitor functions via an MDIO bus. Upon module initialization, these functions are available. The CFP8 MDIO electrical interface consists of four pins including 2pins for MDC and MDIO, the Module Select pin and the Global Alarm pin. MDC is the MDIO Clock line driven by the host and MDIO is the bidirectional data line driven by both the host and module depending upon the data direction. The CFP8 MDIO pins are listed in Table 2-3. Specifications of the CFP8 hardware management interface pins are given in Ref. [2] with the following changes listed below.

Table 2-3: Management Interface Pins (MDIO)

Pin #	Symbol	Description	I/O	Logic	“H”	“L”	Pull-up /down
89	GLB_ALRMn	Global Alarm	O	3.3V LVCMOS	OK	Alarm	
92	MDC	MDIO Clock	I	1.2V LVCMOS			
91	MDIO	Management Data Input Output Bi-Directional Data	I/O	1.2V LVCMOS			
90	MOD_SELn	Module Select	I	3.3V LVCMOS	De-select	Select	Pull-Up ³

³ Pull-Up resistor (4.7 kOhm to 10 kOhm) is located within the CFP8 module

For CFP8, the MOD_SELn pin replaces the PRTADR pins used on CFP/CFP2/CFP4. The MOD_SELn pin is used in cases where a single MDIO bus is shared between more than one CFP8 module.

2.5.1 **Baseline MDIO Arrangement (Required)**

The baseline arrangement has a separate MDIO bus (MDC and MDIO) for each CFP8 module. In this case, the MOD_SELn pin is unused by the CFP8 module and can be a “no connect” on the host. The host addresses each CFP8 module using the power-up and reset default. See 3.1 for more details.

2.5.2 Optional MDIO Arrangement

In systems where a single MDIO bus (MDC and MDIO) is shared between multiple CFP8 modules, the MOD_SEL_n pins override the internal CFP8 module address. When MOD_SEL_n is asserted low, the CFP8 module responds to any address. This enables the host to write unique module addresses to each CFP8 module. See 3.2 for more details.

2.6 CFP8 MANAGEMENT INTERFACE HARDWARE DESCRIPTION

Per specifications given in Ref. [2].

2.7 HARDWARE SIGNALING PIN ELECTRICAL SPECIFICATIONS

2.7.1 Control & Alarm Pins: 3.3V LVCMOS Electrical Characteristics

The hardware control and alarm pins specified as 3.3V LVCMOS functionally described above shall meet the characteristics described in Ref. [1]. Reference figures are provided regarding pin termination; see Figure 2-1 and Figure 2-2.

Figure 2-1: Reference +3.3V LVCMOS Output Termination

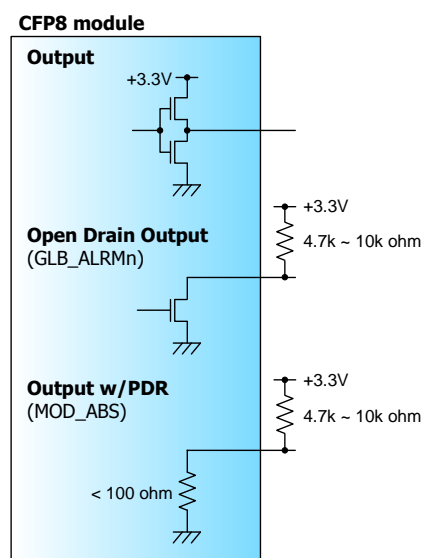
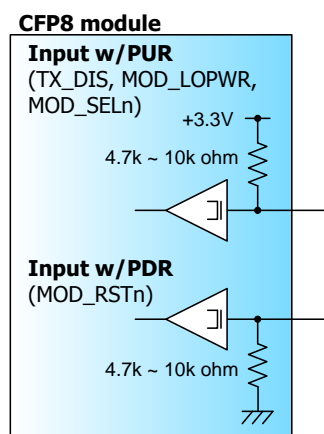


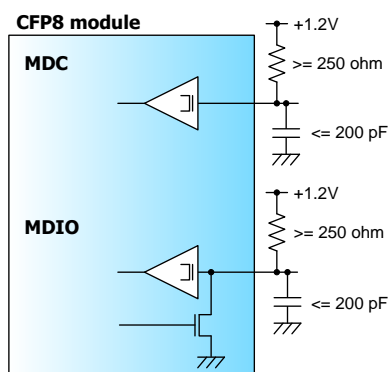
Figure 2-2: Reference 3.3V LVCMOS Input Termination



2.7.2 MDIO Interface Pins: 1.2V LVCMOS Electrical Characteristics

The MDIO interface pins specified as 1.2V LVCMOS functionally described above shall meet the characteristics described in Ref. [1]. Reference figure is provided regarding pin termination; see Fig.2-3.

Figure 2-3: Reference MDIO Interface Termination²



² The MSA recommends host termination resistor value of 560 Ohms, which provides the best balance of performance for both open-drain and active tri-state driver in the module. Host termination resistor values below 560Ohms are allowed, to a minimum of 250 Ohms, but this degrades active driver performance. Host termination resistor values above 560 Ohms are allowed but this degrades open-drain driver performance.

The above drawings, with maximum host load capacitance of 200pF, also define the measurement set-up for module MDC timing verification. The capacitor in the drawing indicates the stray capacitance on the line. Don't put any physical capacitor on the line.

2.8 HARDWARE SIGNALING PIN TIMING REQUIREMENTS

Per specifications given in Ref. [2]

2.8.1 *Optional MOD_SELn Timing Requirements*

The addition of the MOD_SELn input pin to CFP8 requires a new timing specification, not covered by reference [4]. A timing diagram is shown in Figure 2-4. The timing parameters are listed in Table 2-4.

Figure 2-4: Optional MOD_SELn Timing Diagram

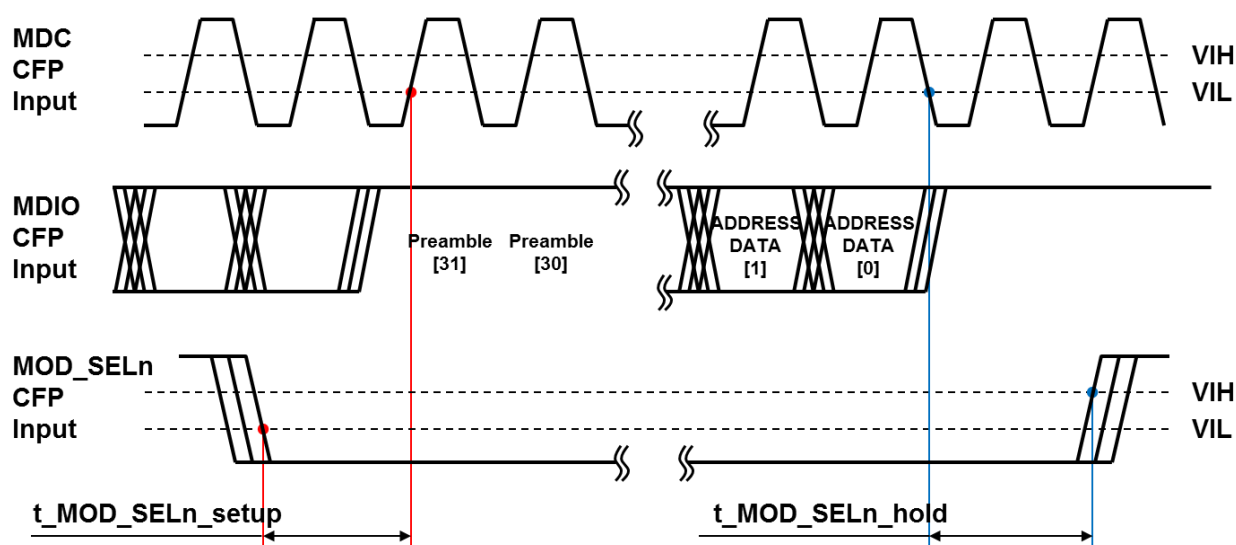


Table 2-4: Optional MOD_SELn Timing Parameters

Parameter	Symbol	Min.	Max.	Unit	Notes & Condition
Host MOD_SELn Setup Time	$t_{MOD_SELn_setup}$	100	-	ms	Before the rising edge of MDC clock cycle for the first preamble bit.
Host MOD_SELn Hold Time	$t_{MOD_SELn_hold}$	1	-	ms	After the falling edge of MDC clock cycle for the last ADDRESS/DATA bit.

3 MODULE MANAGEMENT INTERFACE DESCRIPTION

The CFP8 module utilizes MDIO IEEE Std. 802.3™-2015 clause 45 [6] for its management interface. The CFP8 MDIO implementation is defined in a separate document entitled, “CFP MSA Management Interface Specification” [4].

Because CFP8 has the MOD_SEL_n pin instead of PRTADR pins, the following describes the CFP8 addressing and startup requirements.

3.1 BASELINE: DEDICATED MDIO BUS PER CFP8 MODULE

The initial PHYADR value in CFP8 is 5b'00000. The CFP8 module comes out of power-up or reset with the default address and responds to any MDIO command with this default address.

Host intervention is not required. The MOD_SEL_n pin is unused by the CFP8 module and can be a ‘no connect’ on the host.

3.2 OPTIONAL: MDIO BUS SHARED BETWEEN MULTIPLE CFP8 MODULES

The initial PHYADR value in CFP8 is 5b'00000. The CFP8 module comes out of power-up or reset with the default address and responds to any MDIO command

Hosts that use a shared MDIO bus need to assert MOD_SEL_n individually³ to set the module addresses as follows:

1. The host asserts MOD_SEL_n before setting a new PHYADR to a target CFP8.
2. When the host asserts the MOD_SEL_n pin, the CFP8 module responds to any operation code (i.e. OP=00 or 01 or 10 or 11) on the MDIO bus⁴. Any PHYADR is valid. The CFP8 PHYADR is changed to the received PHYADR.

³ MOD_SEL_n asserted means that the MOD_SEL_n pin is set low and the module is selected. MOD_SEL_n de-assert means that the MOD_SEL_n pin is set high and the module is de-selected.

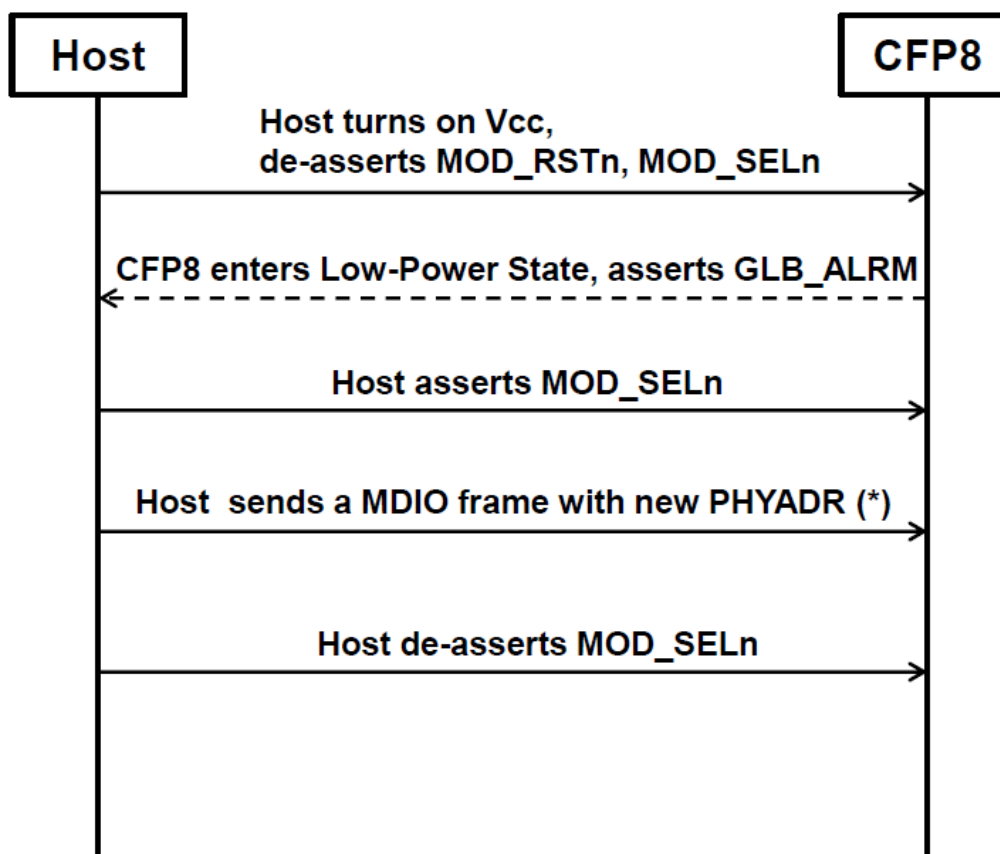
⁴ When MOD_SEL_n is asserted, data following PHYADR (i.e. DEVADR, TA and 16-bit ADDRESS/DATA) is neglected regardless of the operation code.

- Once the new PHYADR is stored, the CFP8 retains the PHYADR until power-off, reset or reprogramming during the next MOD_RSTn assertion.

WARNING: In the optional shared MDIO implementation, when a CFP8 module comes out from power-up or reset, including after hot-plug into an operating host, the host must ensure that there is no bus contention conflict. For example, the host cannot use default address 5b'00000 for normal traffic because it will result in multiple modules responding.

The PHYADR setup sequence for host systems with the optional shared MDIO bus configuration is illustrated in Figure 3-1.

Figure 3-1 PHYADR Setup Sequence for Optional Shared MDIO bus



(*) With any operation code; 00/01/10/11.

4 PERFORMANCE SPECIFICATIONS

4.1 OPERATING ENVIRONMENT

Per specifications given in Ref. [1]

4.2 POWER SUPPLIES AND POWER DISSIPATION

4.2.1 *Voltage power supply and power dissipation*

The CFP8 module power supply and maximum power dissipation specifications are defined in Table 4-1.

4.2.2 *Inrush current*

The inrush current on the 3.3V power supply shall be limited by the CFP8 module to assure a maximum rate of change defined in Table 4-1.

4.2.3 *Turn-off current*

The CFP8 module shall limit the turn-off current to assure a maximum rate of change per Table 4-1.

4.2.4 *Power Supply Noise Susceptibility*

A host system will supply stable power to the module and guarantee that noise & ripple on the power supply does not exceed that defined in Table 4-1. A possible example of a power supply filtering circuit that might be used on the host system is a PI C-L-C filter. A module will meet all electrical requirements and remain fully operational in the presence of noise on the 3.3V power supply which is less than that defined in the table 4-1. The component values of a power supply noise filtering circuit, such as the capacitor and inductor, must be selected such that maximum Inrush and Turn-off current does not cause voltage transients which exceed the absolute maximum power supply voltage, all specified in Table 4-1.

Table 4-1: Voltage Power Supply

Parameters		Symbol	Min	Typ.	Max	Unit
Absolute Maximum Power Supply Voltage		VCC	-	-	3.6	V
Total Power Dissipation	Class 1	Pw	-	-	4	W
	Class 2		-	-	8	
	Class 3		-	-	12	
	Class 4		-	-	16	
	Class 5		-	-	20	
	Class 6		-	-	24	
Low Power Mode Dissipation		Plow	-	-	2	W
Operating Power Supply Voltage		VCC	3.2	3.3	3.4	V
Operating Power Supply Current ¹	Class 1 and 2	ICC	-	-	2.5	A
	Class 3 and 4		-	-	5	
	Class 5 and 6		-	-	7.5	
Inrush Current ²	Class 1 and 2	I-inrush	-	-	150	mA/usec
Turn-off Current		I-turnoff	-150	-	-	
Inrush Current ²	Class 3 and 4	I-inrush	-	-	300	
Turn-off Current		I-turnoff	-300	-	-	
Inrush Current ²	Class 5 and 6	I-inrush	-	-	450	
Turn-off Current		I-turnoff	-450	-	-	
Power Supply Noise		Vrip	-	-	2% 3%	DC – 1MHz 1 – 10MHz

¹ Maximum current per pin shall not exceed 800 mA. Those power classes for which the maximum current per pin exceeds 800 mA will require agreement from an electrical connector supplier.

² For modules which present a small capacitive load to the host during hot plug ($C \leq 500$ nF), the portion of the inrush current due to charging the capacitor can be excluded from the total inrush current which must meet the maximum limit specification.

4.2.5 Grounding

Per specifications given in Ref. [1].

4.3 OPTICAL CHARACTERISTICS

4.3.1 Optical Specifications

The CFP8 module will comply with standardized optical specifications such as the optical reaches specified in IEEE for datacom applications or in ITU-T for telecom applications. Some of the relevant reference documents are: IEEE Std. 802.3TM-2015, and working drafts of IEEE P802.3bs.

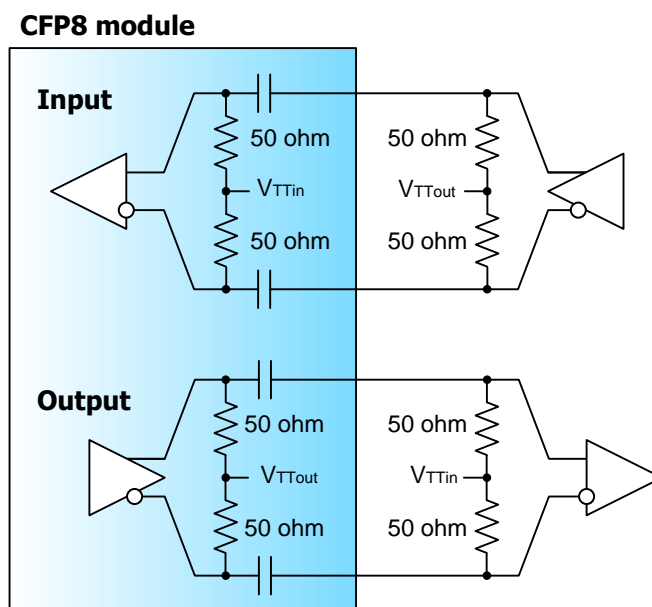
4.4 HIGH SPEED ELECTRICAL CHARACTERISTICS

The CFP8 Module high speed electrical interface supports the following configurations:

- 1) 16 tx lanes + 16 rx lanes, each at 25.78125 Gb/s NRZ;
- 2) 16 tx lanes + 16 rx lanes, each at 26.5625 Gb/s NRZ;
- 3) 8 tx lanes + 8 rx lanes, each at 26.5625 GBd PAM-4.

The high speed electrical interface shall be AC-coupled within the CFP8 module as is shown in Figure 4-1.

Figure 4-1: High Speed I/O for Data and Clocks



4.4.1 25.78125 Gb/s NRZ Transmitter Data (and Clock)

The 25.78125 Gb/s NRZ Transmitter Data is defined in IEEE Std. 802.3 Annex 83E for CAUI-4 chip-to-module, with the exception that the CFP8 supports up to 16 lanes. Figure 4-1 shows the recommended termination for these circuits. Lane orientation and designation is specified in the pin-map tables given in Section 5.

4.4.2 25.78125 Gb/s NRZ Receiver Data (and Clock)

The 25.78125 Gb/s NRZ Receiver Data is defined in IEEE Std. 802.3 Annex 83E for CAUI-4 chip-to-module, with the exception that the CFP8 supports up to 16 lanes. Figure 4-1 shows the recommended termination for these circuits. Lane orientation and designation is specified in the pin-map tables given in Section 5

4.4.3 26.5625 Gb/s NRZ Transmitter Data (and Clock)

The 26.5625 Gb/s NRZ Transmitter Data is defined in IEEE P802.3bs Annex 120C for 400GAUI-16 chip-to-module. Figure 4-1 shows the recommended termination for these circuits. Lane orientation and designation is specified in the pin-map tables given in Section 5.

4.4.4 26.5625 Gb/s NRZ Receiver Data (and Clock)

The 26.5625 Gb/s NRZ Receiver Data is defined in IEEE P802.3bs Annex 120C for 400GAUI-16 chip-to-module. Figure 4-1 shows the recommended termination for these circuits. Lane orientation and designation is specified in the pin-map tables given in Section 5

4.4.5 26.5625 GBd PAM-4 Transmitter Data (and Clock)

The 26.5625 GBd PAM-4 Transmitter Data is defined in IEEE P802.3bs Annex 120E for 400GAUI-8 chip-to-module. Figure 4-1 shows the recommended termination for these circuits. Lane orientation and designation is specified in the pin-map tables given in Section 5.

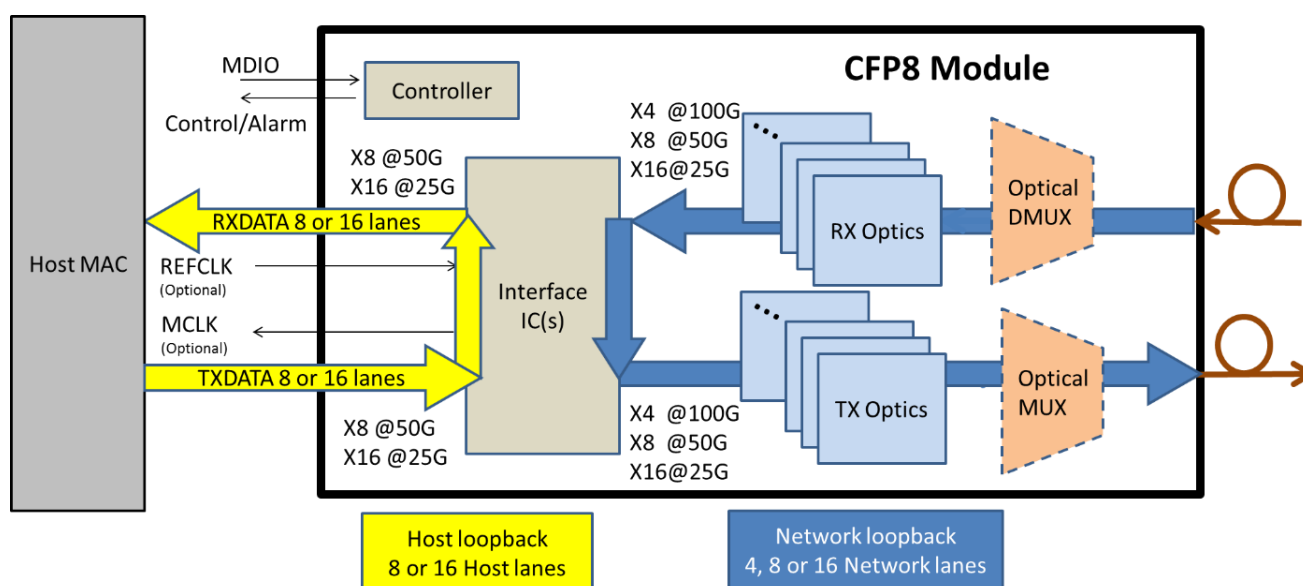
4.4.6 26.5625 GBd PAM-4 Receiver Data (and Clock)

The 26.5625 GBd PAM-4 Receiver Data is defined in IEEE P802.3bs Annex 120E for 400GAUI-8 chip-to-module. Figure 4-1 shows the recommended termination for these circuits. Lane orientation and designation is specified in the pin-map tables given in Section 5.

4.4.7 Loopback (Optional)

The CFP8 module may optionally support loopback functionality. Loopback commands are accessed via the MDIO management interface. Recommended loopback orientation implementation is TX0 to RX0. The host loopback and the network loopback are oriented per Figure 4-2 shown below. The capability to support the loopback functionality is dependent upon the interface IC technology, labeled as “Interface IC(s)” block in the figure. The CFP MSA module vendor will specify which loopback functionality, if any, is supported. For details on controlling the loopback mode, please refer to Ref. [4].

Figure 4-2: CFP8 Module Optional Loopback Orientation



4.4.8 Reference Clock (Optional)

For 16 x 26.5625 Gb/s or 8 x 26.5625 GBd PAM-4 (1 x 400 GbE) host electrical interface applications, the host may supply a reference clock (REFCLK) at 1/170 electrical lane rate. The CFP8 module may use the 1/170 reference clock for transmitter path retiming, for example for Datacom applications.

For 16 x 25.78125 Gb/s (4 x 100 GbE) host electrical interface applications, the host may supply a reference clock (REFCLK) at 1/160 electrical lane rate. The CFP8 module may use the 1/160 reference clock for transmitter path retiming, for example for Datacom applications.

When provided, the REFCLK shall be CML differential AC-coupled and terminated within the CFP8 module as shown in Table 4-2. There is no required phase relationship between the data lanes and the reference clock, but the clock frequency shall not deviate more than specified in Table 4-2. For detailed clock characteristics please refer to the below table.

Table 4-2: Optional Reference Clock Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Impedance	Zd	80	100	120	Ω	
Frequency						See Table 4-4.
Frequency Stability	Δf	-100		100	ppm	For Ethernet applications;
		-20		20		For Telecom applications
Input Differential Voltage	VDIFF	400		1200	mV	Peak to Peak Differential
RMS Jitter ^{1,2}	σ			10	ps	Random Jitter over frequency band of 10kHz < f < 10MHz
Clock Duty Cycle		40		60	%	
Clock Rise/Fall Time 10/90%	tr/f	200		1250	ps	1/160 of electrical lane rate for 25.78125 Gb/s NRZ per lane module and 1/170 of electrical lane rate for 26.5625 Gb/s NRZ or 26.5625 GBd PAM-4 per lane module.
		50		315		1/40 of electrical lane rate for 25.78125 Gb/s NRZ per lane module and TBD of electrical lane rate for 26.5625 Gb/s NRZ or 26.5625 GBd PAM-4 per lane module.

¹ The spectrum of the jitter within this frequency band is undefined. The CFP8 shall meet performance requirements with worst case condition of a single jitter tone of 10 ps RMS at any frequency between 10 kHz and 10 MHz

² For Telecom applications better jitter may be required.

An example of CFP8 clocking for 16 x 25 Gb/s applications is shown in Figure 4-3. An example of CFP8 clocking for 8 x 50 Gb/s PAM-4 applications is shown in Figure 4-4.

4.4.9 Transmitter Monitor Clock (Optional)

Not specified in this document. See 4.4.11.

4.4.10 Receiver Monitor Clock (Optional)

Not specified in this document. See 4.4.11.

4.4.11 Monitor Clock (Optional)

The CFP8 module may supply either a transmitter monitor clock or a receiver monitor clock for 16 x 25 Gb/s or for 8 x 50 Gb/s PAM-4 applications. The monitor clock is intended to be used as a reference for measurements of the optical input or output. If provided, the clock shall operate at a rate relative to the host electrical lane rate of 1/8 or 1/48 or 1/64 of 26.5625 GBd host lane rates. For host lane rates of 25.78125 Gb/s, MCLK can operate at 1/8, 1/32, 1/40 or 1/160 of the host lane rate as listed in Table 4-4. When provided, the MCLK shall be CML differential AC-coupled and terminated within the CFP8 module as shown in Figure 4-1. Detailed clock characteristics are specified in Table 4-3.

The user can select the source of the Monitor clock. MDIO register bits to select the source of MCLK for the CFP8 module are located in the VR region. Please refer to Ref. [4] for details.

Table 4-3: Optional Monitor Clock Characteristics

		Min.	Typ.	Max.	Unit	Notes
Impedance	Zd	80	100	120	Ω	
Frequency						See Table 4-4
Output Differential Voltage	VDIFF	400		1200	mV	Peak to Peak Differential
Clock Duty Cycle		40		60	%	

Table 4-4: CFP8 Module Clocking Signals

Clock Name	Status	I/O	M x 26.5625 Gb/s NRZ or M x 26.5625 GBd PAM-4 Default Host Lane Rate		Optional Rate
			Datacom 400GBASE-SR16/DR4/FR8/LR8	Telecom ?	
REFCLK	Optional	I	1/170 (156.25 MHz)		
MCLK	Optional	O	1/8 (3.3203 GHz) Or 1/48 (553.385 MHz) or 1/64 (415.039 MHz)		
Clock Name	Status	I/O	M x 25 Gb/s Default Host Lane Rate		
			Datacom Up to 4 x 100GBASE-SR4/LR4/ER4	Telecom Up to 4 x OTU4	
REFCLK	Optional	I	1/160 (161.1328 MHz) or 1/40 (644.5313 MHz)	1/160 (174.7031 MHz) or 1/40 (698.8123 MHz)	
MCLK	Optional	O	1/8 (3.2266 GHz) or 1/32 (805.665 MHz) or 1/40 (644.5313 MHz) or 1/160 (161.1328 MHz)	1/8 (3.49406 GHz) or 1/32 (873.515 MHz) or 1/40 (698.8123 MHz) or 1/160 (174.7031 MHz)	

Figure 4-3: Example of Clocking for 16 x 25 Gb/s CFP8 Applications

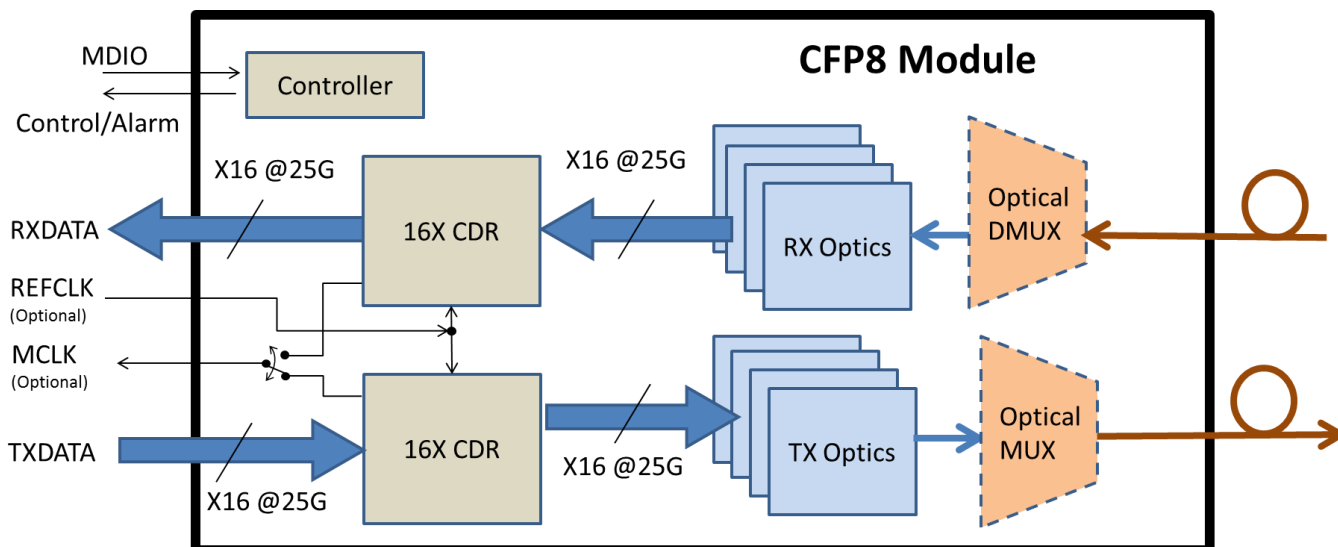
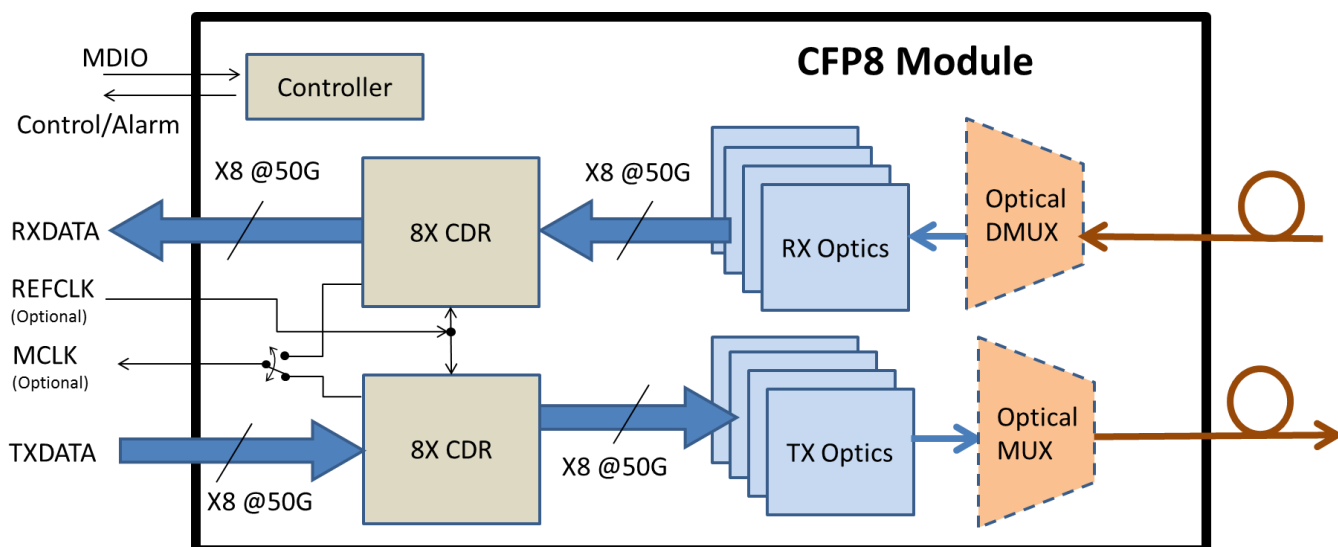


Figure 4-4: Example of Clocking for 8 x 50 Gb/s PAM-4 CFP8 Applications



5 MECHANICAL SPECIFICATIONS

5.1 MECHANICAL OVERVIEW

The CFP8 module is designed to be plugged into a host cage assembly with a riding heat sink. The cage assembly is fabricated within the host system and the CFP8 module may be inserted at a later time. Shown in Figure 5-1 is a drawing of the CFP8 module and CFP8 modules inserted into a host single- or dual-port cage system with a riding heat sink. The riding heat sinks in Figure 5-1 need to be oriented for the system airflow direction, either side-to-side or front-to-back.

Figure 5-1: CFP8 Module & CFP8 Module Mated in Single and Dual Port Systems

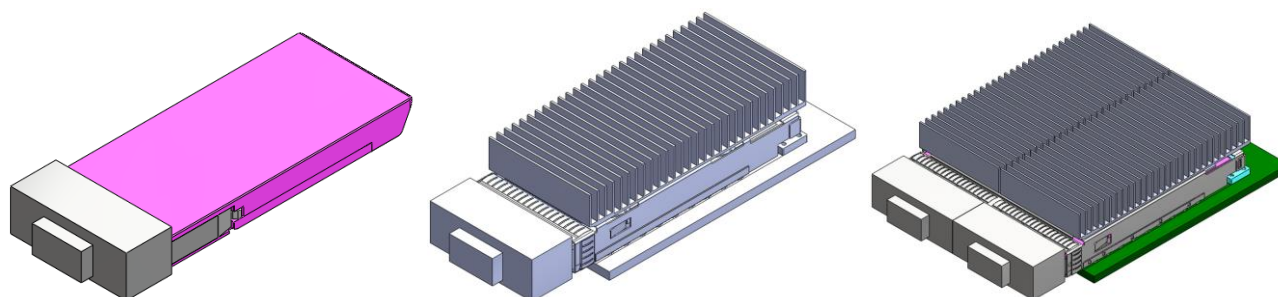
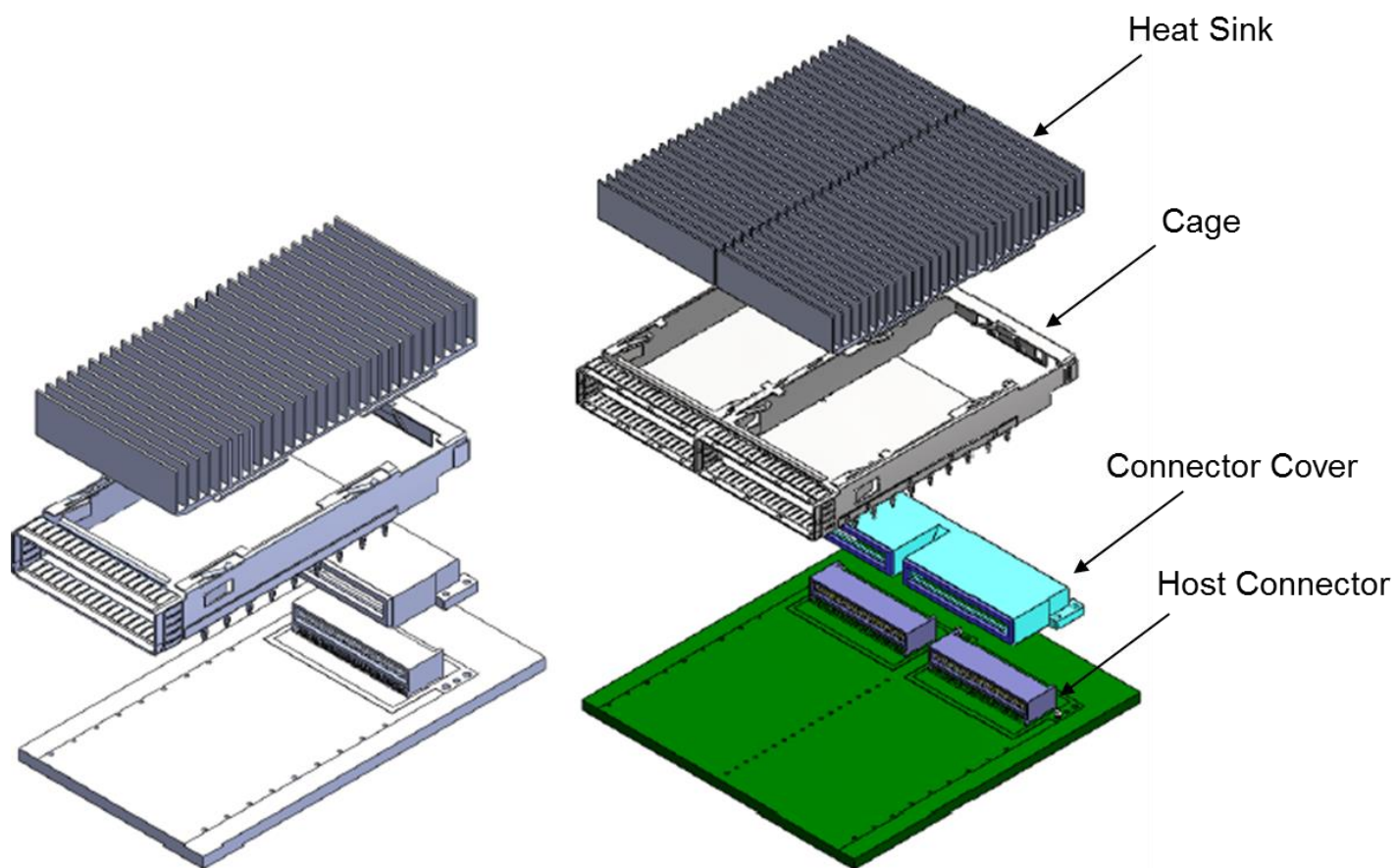


Figure 5-2 is an overview of the CFP8 mechanical assembly of the constituent elements. The detailed dimensions are located in a separate design document hosted on the CFP MSA Website (www.cfp-msa.org).

Figure 5-2: Host Cage System and Mounting Method Overview



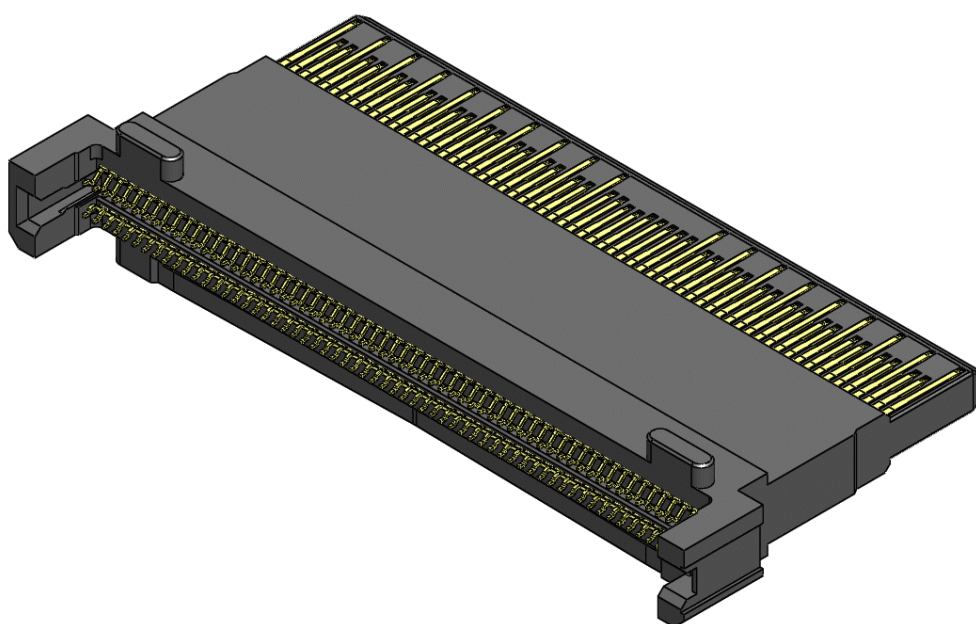
5.2 ELECTRICAL CONNECTOR

Shown below are details of the electrical connector system used for the CFP8 MSA. The detailed dimensions are located in a separate document hosted on the CFP MSA Website (www.cfp-msa.org).

5.2.1 *Module Plug Connector*

The CFP8 MSA specifies a two-piece electrical connector for superior electrical performance and superior mechanical integrity. Shown in Figure 5-3 is the module plug connector assembly which is contained as a sub-component within the CFP8 module.

Figure 5-3: CFP8 Module Plug Connector Assembly



5.2.2 Host Connector

The CFP8 MSA specifies a two-piece electrical connector for superior electrical performance and superior mechanical integrity. Shown in Figure 5-4 and Figure 5-5 are overview drawings of the host connector cover and the host connector assembly. These assemblies shall be built into the host system. The Host Connector shall be covered by the Host Connector Cover Assembly.

Figure 5-4: CFP8 Single & Double Port Host Connector Cover Assemblies

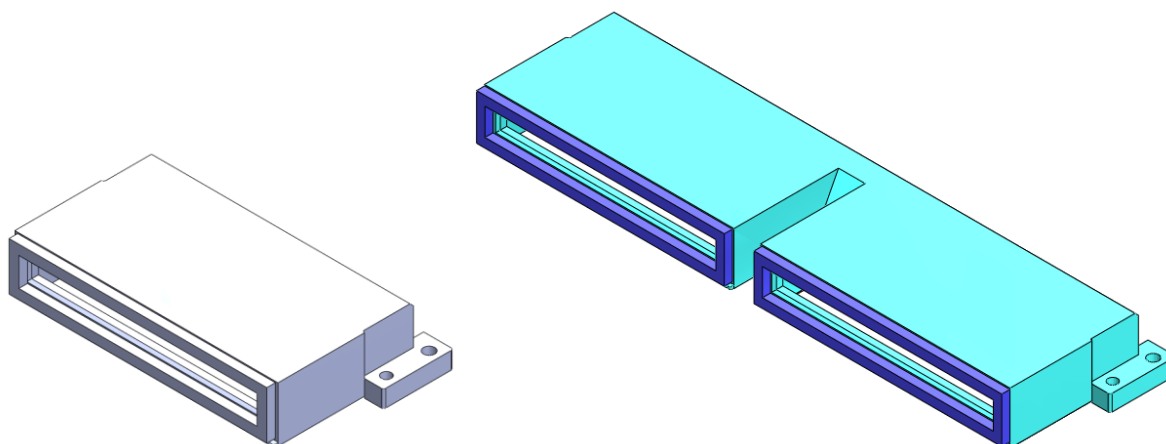
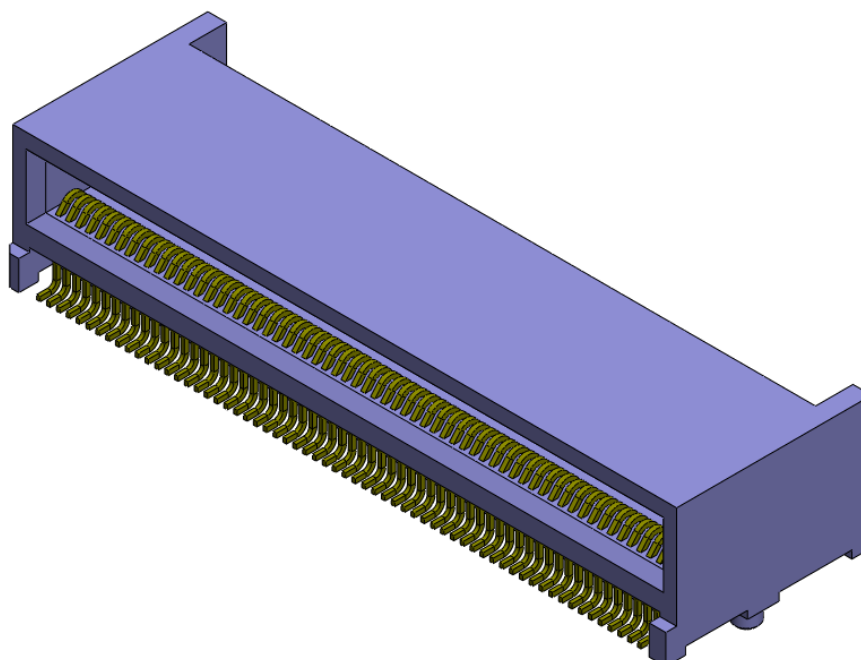


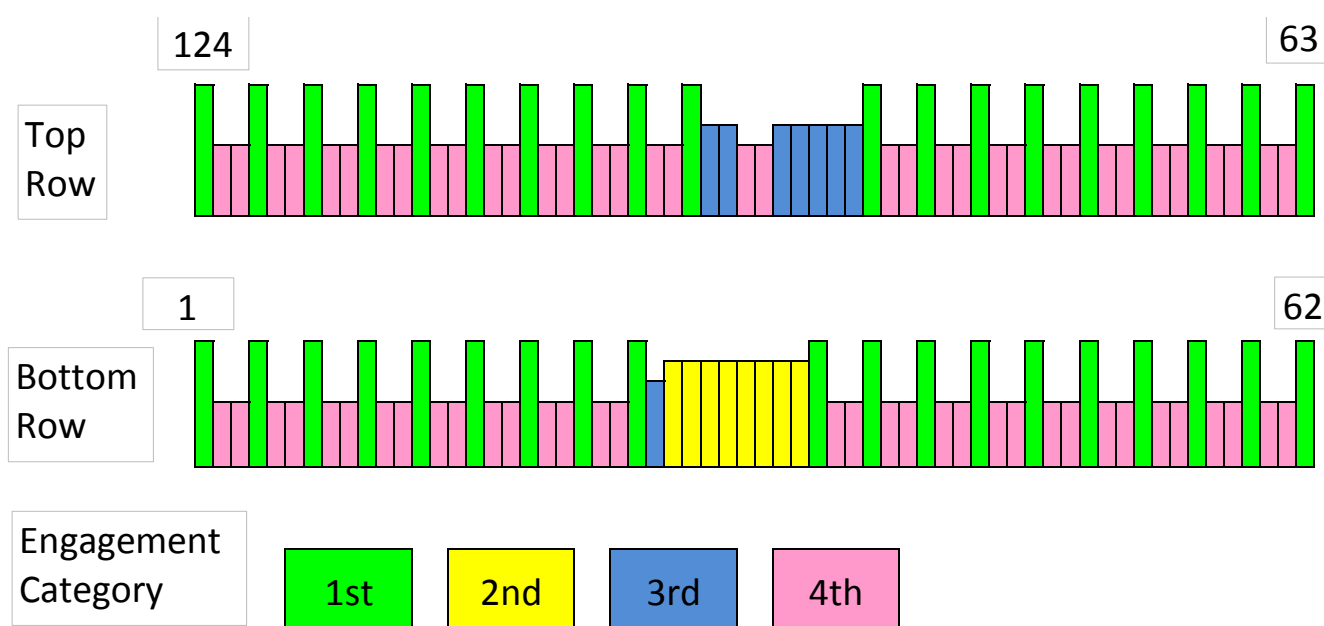
Figure 5-5: CFP8 Host Connector Assembly



5.2.3 Connector Pin Contact Mating

The module plug connector has a physical offset of metal contact pins to insure that certain signals make engagement between the module and host prior to other signals. There are four categories of pin engagement. A map of the connector engagement is shown in Figure 5-6. The connector pin map engagement order is guaranteed by the physical offset built into the module plug connector. The host connector has all contacts on the same plane without offset.

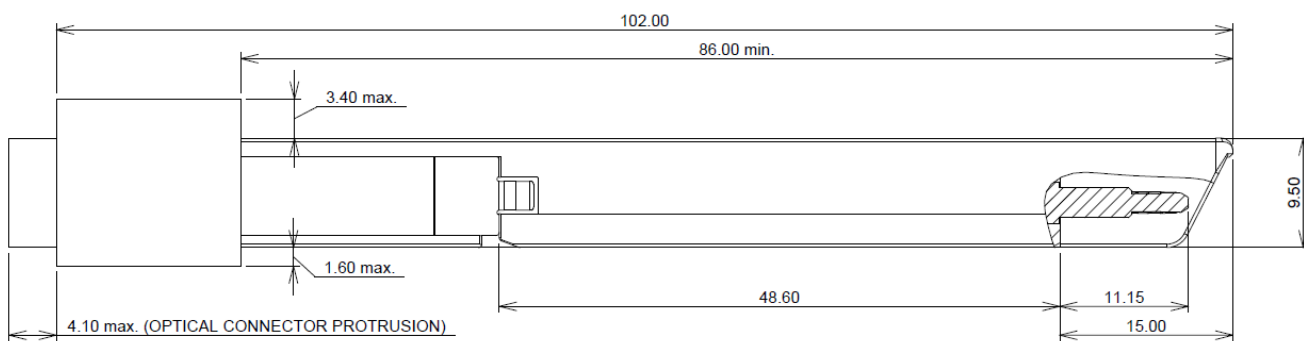
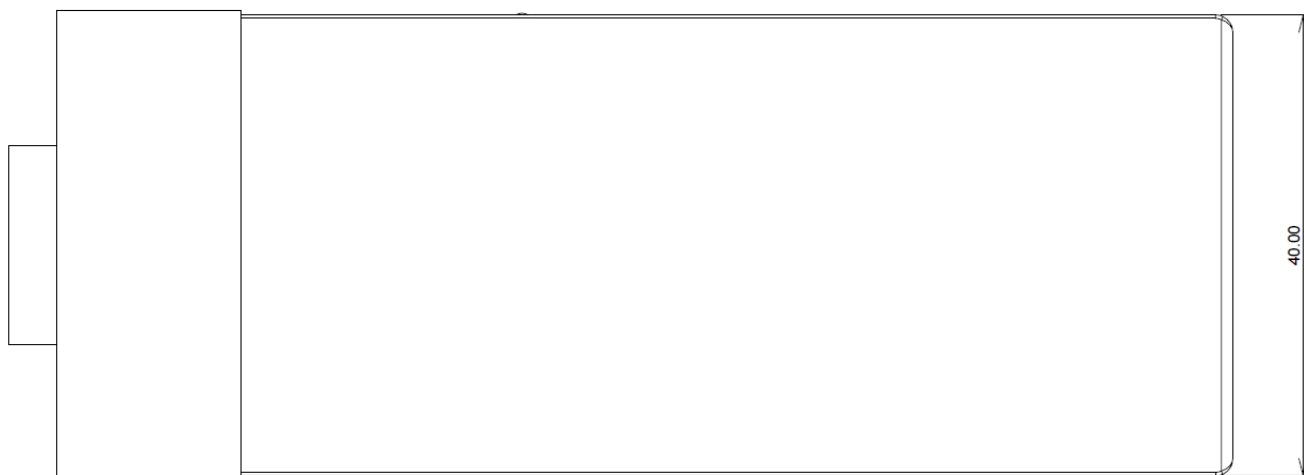
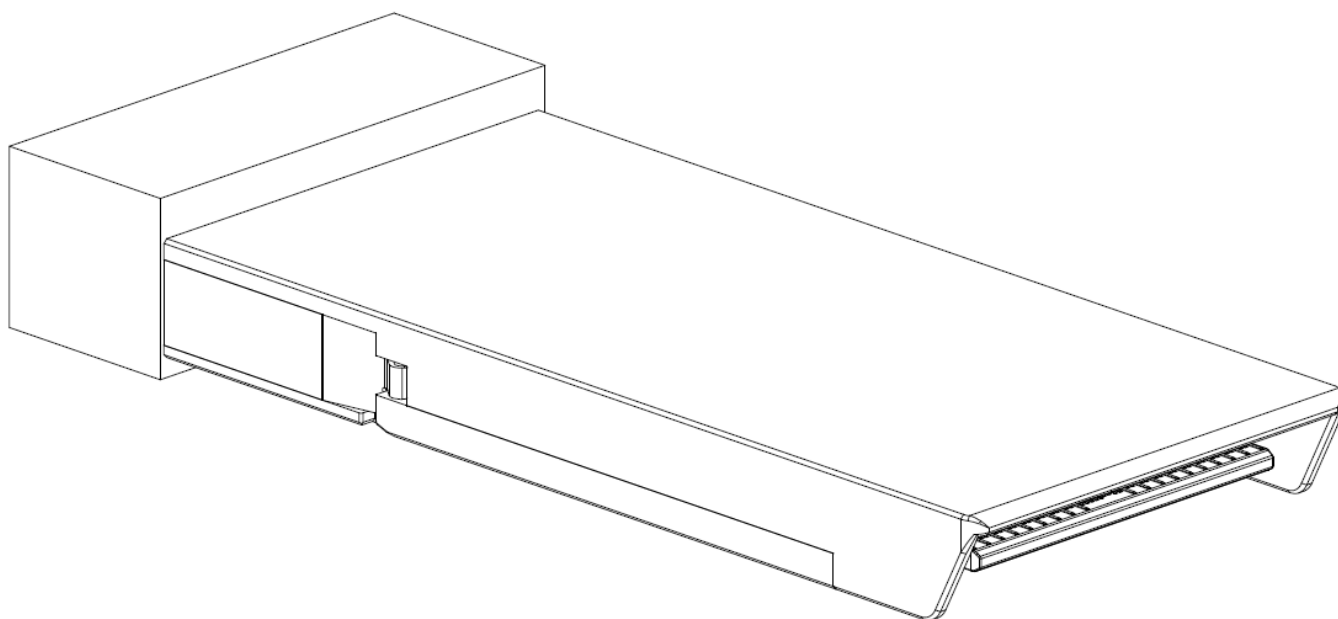
Figure 5-6: CFP8 Pin Map Connector Engagement



5.3 CFP8 MODULE DIMENSIONS

An overview of the CFP8 module dimensions is shown in the below Figure 5-7. The CFP8 maximum header height is specified as shown in Figure 5-7. The detailed CFP8 module dimensions are located in a separate document hosted on the CFP MSA Website (www.cfp-msa.org). All mechanical hardware dimensions in this document are for reference only. Normative dimensions are found in the latest published CFP8 baseline drawing.

Figure 5-7: CFP8 Module Dimension Overview



5.3.1 CFP8 Mechanical Surface Characteristics

The mechanical surface of flat top CFP8 module which may be in contact with the host riding heat sink assembly shall be compliant with specifications in Table 5-1. The parameters listed in Table 5-1 define the CFP8 module thermal interface and may be used by host system designers to specify the host cage assembly opening and riding heat sink for optimizing host system thermal management performance. Surface flatness and roughness parameters are specified per CFP8 module power class (see Table 5-1) to allow for optimization of module thermal performance and cost. Non-compliance to these specifications may cause significant thermal performance degradation. Only the top surface of the module is assumed to be used for heat transfer.

Table 5-1: CFP8 Mechanical Characteristics

Parameters	Power Class	Min.	Max.	Unit	Notes
Weight	1 – 6		210	g	
Flatness	1		0.15	mm	
	2		0.15	mm	
	3		0.12	mm	
	4		0.12	mm	
Roughness	1		3.2	Ra	
	2		3.2	Ra	
	3		1.6	Ra	
	4		1.6	Ra	
Temperature Delta	1 - 4		7	°C	No heat sink; 200 lfm sideways airflow
Normal force exerted on module	1 - 4	5	15	N	Heat sink on module top surface

5.3.2 CFP8 Insertion & Extraction

As described in Section 1, the CFP8 module shall be hot pluggable. A consequence of the CFP8 module being hot pluggable is that an end user be equipped to insert and extract the module in the field. The required forces are specified below in Table 5-2.

Table 5-2: CFP8 Module Insertion, Extraction Forces

	Max.	Unit	Notes
Maximum Insertion Force	80	N	Without Heat Sink
Maximum Extraction Force	50	N	Without Heat Sink
Minimum Module Retention Force	90	N	No damage to module below 90 N
Minimum Cage Retention Force	180	N	No damage to cage latch below 180 N

Minimum rating for host/module connector insertion/extraction is 200 cycles.

* Typical increase in those forces by adding heat sink is below 5N.

5.4 HOST SYSTEM DIMENSIONS

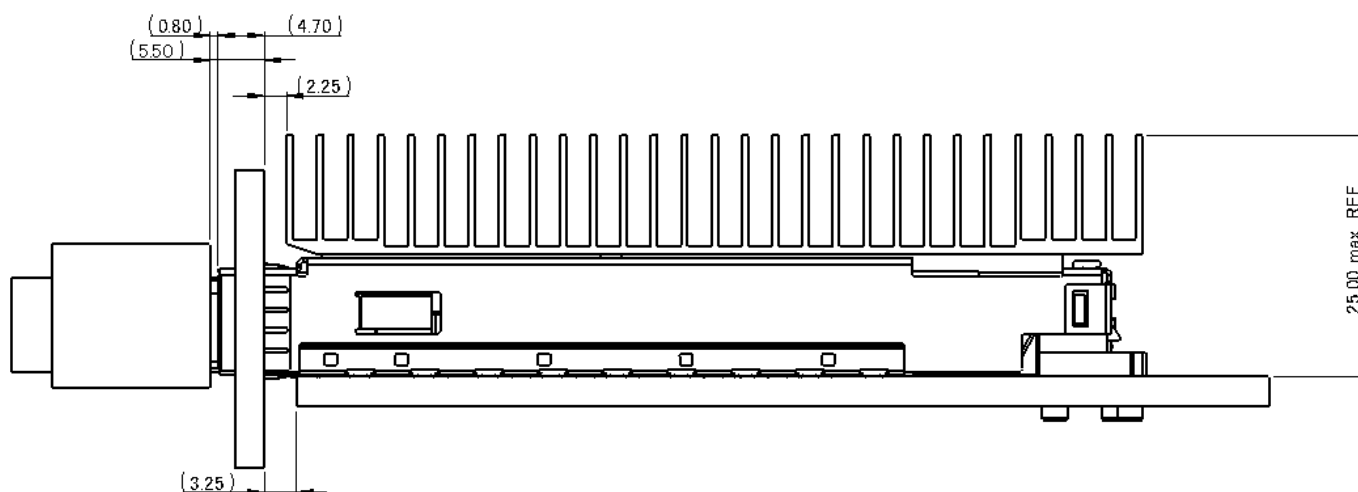
The detailed CFP8 host system dimensions including host board layout are located in a separate document hosted on the CFP MSA Website (www.cfp-msa.org).

5.5 RIDING HEAT SINK

The riding heat sink and host cage top surface designs given in the latest published CFP8 baseline drawing are only exemplary and are not required for compliance with the CFP8 MSA. Cage opening and heat sink specifications vary with host system design and thermal performance requirements. The heat sink/cage designs are therefore host system dependent and may be optimized by the system designer.

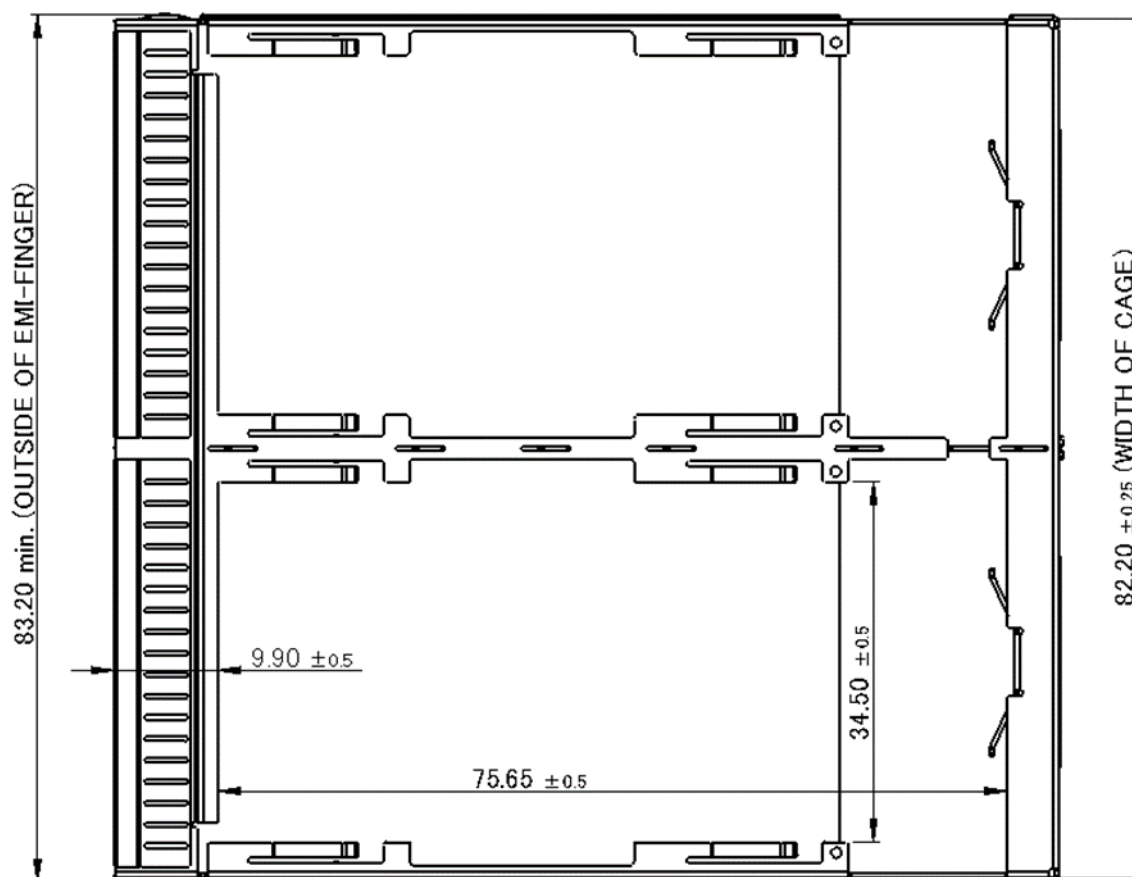
The riding heat sink illustrated in Figure 5-8 is for example only. The recommended material for the heat sink is aluminum.

Figure 5-8: Riding Heat Sink



The mounting dimensions for the Riding Heat Sink are shown below in Figure 5-9. The actual dimensions of the heat sink and cage top opening may be optimized for the particular host system.

Figure 5-9: Host Cage Top Surface Opening



5.6 OPTICAL CONNECTORS

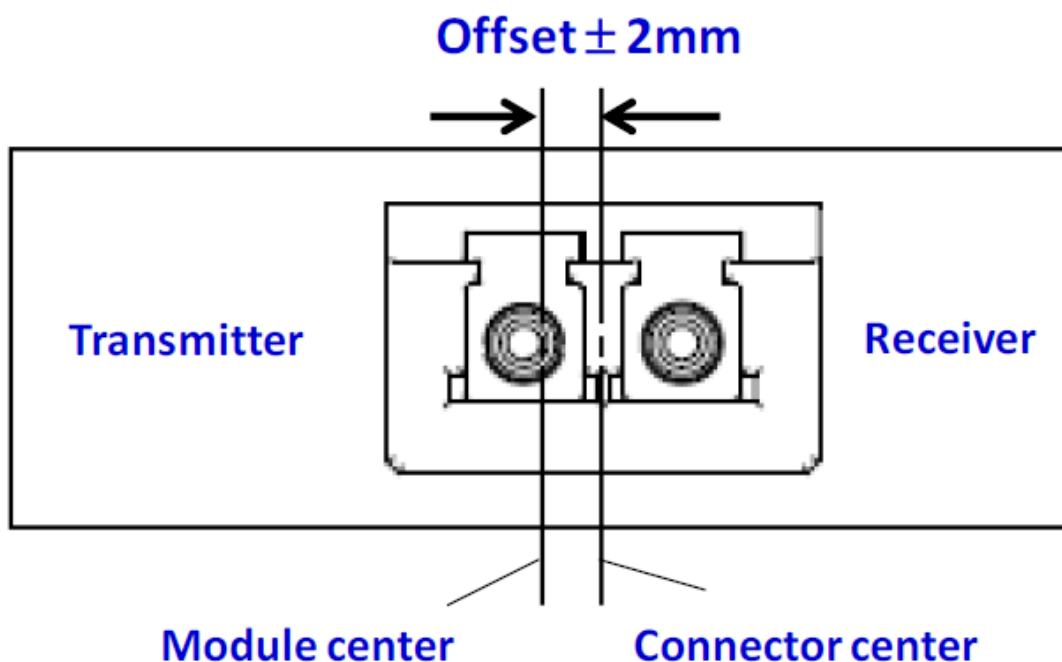
The CFP8 module shall support LC, MTP12 and MTP16 optical connector types, as listed in Table 5-3. The optical connectors are positioned in the CFP8 module as illustrated in Figure 5-10.

Table 5-3: Optical Connectors⁵

Pin #	Category	Reference Number
LC Connector	TBA	TBA
MPO12 Connector	TBA	TBA
MPO16 Connector	TBA	TBA
MPO32 Connector	TBA	TBA

⁵ Other optical connectors may be supported

Figure 5-10: CFP8 Optical Connector Position



5.6.1 Optional Optical LC Connector Position for Telecom Applications

Not supported in the CFP8 module.

5.7 ELECTRICAL CONNECTORS

CFP8 host electrical connector supplier information will be added to Table 5-4 in a future release of this MSA.

Table 5-4: CFP8 Host Connector Assembly

Part Number	Supplier	Part Name
TBA	TBA	Cage
TBA	TBA	Host Connector Cover Assembly
TBA	TBA	Host Connector

5.8 PIN ASSIGNMENT

The CFP8 connector has 124 pins which are arranged in Top and Bottom rows. The CFP8 connector supports the following configurations:

Up to sixteen (16) 25Gbit/s TX lanes plus up to sixteen (16) 25Gbit/s RX lanes;

The CFP8 pin-orderings are shown in Table 5-5. The CFP8 TOP pin-out definition uses the same pin-ordering convention as CFP, CFP2 and CFP4. All modules must support the baseline TOP pin-out definition.

Detailed description of the bottom row pins 1 through pin 62 are given in Table 5-6. Note the REFCLK pins are located on the top row. A single-ended REFCLK is an option. The CFP8 connector pin map orientation is shown in Figure 5-11.

Figure 5-11: CFP8 Connector Pin Map Orientation

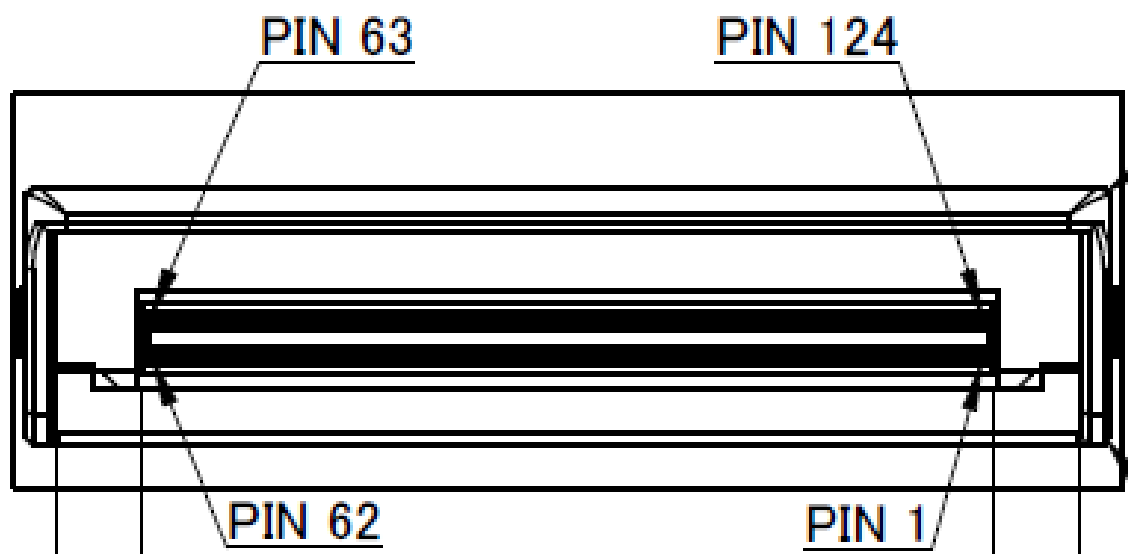


Table 5-5: CFP8 Pin Map

	CFP8 Bottom			CFP8 Top
1	GND		124	GND
2	TX15n		123	TX14n
3	TX15p		122	TX14p
4	GND		121	GND
5	TX13n		120	TX12n
6	TX13p		119	TX12p
7	GND		118	GND
8	TX11n		117	TX10n
9	TX11p		116	TX10p
10	GND		115	GND
11	TX9n		114	TX8n
12	TX9p		113	TX8p
13	GND		112	GND
14	TX7n		111	TX6n
15	TX7p		110	TX6p
16	GND		109	GND
17	TX5n		108	TX4n
18	TX5p		107	TX4p
19	GND		106	GND
20	TX3n		105	TX2n
21	TX3p		104	TX2p
22	GND		103	GND
23	TX1n		102	TX0n
24	TX1p		101	TX0p
25	GND		100	GND
26	GND (VND_IO_A)		99	REFCLKn (VND_IO_E)
27	3.3V		98	REFCLKp (VND_IO_D)
28	3.3V		97	GND
29	3.3V		96	TX_DIS (PRG_CNTL1)
30	3.3V		95	RX_LOS (PRG_ALRM1)
31	3.3V		94	MOD_LOPWR
32	3.3V		93	MOD_ABS
33	3.3V		92	MDC
34	3.3V		91	MDIO
35	GND		90	MOD_SELn
36	MCLKn (VND_IO_B)		89	GLB_ALRMn
37	MCLKp (VND_IO_C)		88	MOD_RSTn
38	GND		87	GND
39	RX15n		86	RX14n
40	RX15p		85	RX14p
41	GND		84	GND
42	RX13n		83	RX12n
43	RX13p		82	RX12p
44	GND		81	GND
45	RX11n		80	RX10n
46	RX11p		79	RX10p
47	GND		78	GND
48	RX9n		77	RX8n
49	RX9p		76	RX8p
50	GND		75	GND
51	RX7n		74	RX6n
52	RX7p		73	RX6p
53	GND		72	GND
54	RX5n		71	RX4n
55	RX5p		70	RX4p
56	GND		69	GND
57	RX3n		68	RX2n
58	RX3p		67	RX2p
59	GND		66	GND
60	RX1n		65	RX0n
61	RX1p		64	RX0p
62	GND		63	GND

Table 5-6: CFP8 Top Row Pin Descriptions

PIN #	NAME	I/O	Logic	Description
124	GND			Ground
123	TX14n	I	CML	Transmit data input
122	TX14p	I	CML	Transmit data input
121	GND			Ground
120	TX12n	I	CML	Transmit data input
119	TX12p	I	CML	Transmit data input
118	GND			Ground
117	TX10n	I	CML	Transmit data input
116	TX10p	I	CML	Transmit data input
115	GND			Ground
114	TX8n	I	CML	Transmit data input
113	TX8p	I	CML	Transmit data input
112	GND			Ground
111	TX6n	I	CML	Transmit data input
110	TX6p	I	CML	Transmit data input
109	GND			Ground
108	TX4n	I	CML	Transmit data input
107	TX4p	I	CML	Transmit data input
106	GND			Ground
105	TX2n	I	CML	Transmit data input
104	TX2p	I	CML	Transmit data input
103	GND			Ground
102	TX0n	I	CML	Transmit data input
101	TX0p	I	CML	Transmit data input
100	GND			Ground
99	REFCLKn (VND_IO_E)	I/O		In normal use, Pins 98 and 99 are used by the host card to source a REFCLK signal to the module. Optionally, Pins 98 and 99 can be used by test and evaluation cards as VND_IO_D, _E. It is up to the module to properly support this.
98	REFCLKp (VND_IO_D)	I/O		
97	GND			Ground
96	TX_DIS (PRG_CNTL1)	I	LVC MOS w/ PUR	Programmable Control 1 set over MDIO. MSA Default: Transmit Disable for all lanes. "1" or NC: transmitter disabled, "0": transmitter enabled.
95	RX_LOS (PRG_ALRM1)	O	LVC MOS	Programmable Alarm 1 set over MDIO. MSA Default = Receiver Loss of Signal, "1": low signal, "0": normal condition.
94	MOD_LOPWR	I	LVC MOS w/ PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled
93	MOD_ABS	O	PDR to GND	Module Absent. "1": module absent, "0": module present. Pull Up Resistor on Host.
92	MDC	I	1.2V CMOS	Management Data Clock (electrical specs per IEEE Std. 802.3™ -2015)
91	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs per IEEE Std. 802.3™ -2015)
90	MOD_SELn	I	LVC MOS w/ PUR	Module Select. "0": module responds to MDIO bus, "1": module ignores MDIO bus. Pull-up resistor in module.
89	GLB_ALRMn	O	LVC MOS (Open Drain)	Global Alarm. "0": alarm condition in any MDIO alarm register, "1": no alarm condition. Open Drain. Pull Up Resistor on Host.
88	MOD_RSTn	I	LVC MOS w/ PDR	Module Reset. "0": resets the module, "1" or NC: module enabled. Pull Down Resistor in Module.
87	GND			Ground
86	RX14n	O	CML	Received data output
85	RX14p	O	CML	Received data output
84	GND			Ground
83	RX12n	O	CML	Received data output
82	RX12p	O	CML	Received data output
81	GND			Ground

PIN #	NAME	I/O	Logic	Description
80	RX10n	O	CML	Received data output
79	RX10p	O	CML	Received data output
78	GND			Ground
77	RX8n	O	CML	Received data output
76	RX8p	O	CML	Received data output
75	GND			Ground
74	RX6n	O	CML	Received data output
73	RX6p	O	CML	Received data output
72	GND			Ground
71	RX4n	O	CML	Received data output
70	RX4p	O	CML	Received data output
69	GND			Ground
68	RX2n	O	CML	Received data output
67	RX2p	O	CML	Received data output
66	GND			Ground
65	RX0n	O	CML	Received data output
64	RX0p	O	CML	Received data output
63	GND			Ground

Table 5-7: CFP8 Bottom Row Pin Descriptions

PIN #	NAME	I/O	Logic	Description
1	GND			Ground
2	TX15n	I	CML	Transmit data input
3	TX15p	I	CML	Transmit data input
4	GND			Ground
5	TX13n	I	CML	Transmit data input
6	TX13p	I	CML	Transmit data input
7	GND			Ground
8	TX11n	I	CML	Transmit data input
9	TX11p	I	CML	Transmit data input
10	GND			Ground
11	TX9n	I	CML	Transmit data input
12	TX9p	I	CML	Transmit data input
13	GND			Ground
14	TX7n	I	CML	Transmit data input
15	TX7p	I	CML	Transmit data input
16	GND			Ground
17	TX5n	I	CML	Transmit data input
18	TX5p	I	CML	Transmit data input
19	GND			Ground
20	TX3n	I	CML	Transmit data input
21	TX3p	I	CML	Transmit data input
22	GND			Ground
23	TX1n	I	CML	Transmit data input
24	TX1p	I	CML	Transmit data input
25	GND			Ground
26	GND (VND_IO_A)	I/O		In normal use, Pin 26 is tied to GND on the host card. Optionally, Pin 26 can be used by test or evaluation cards as VND_IO_A. It is up to the module to properly support this.
27	3.3V			3.3V Module Supply Voltage
28	3.3V			3.3V Module Supply Voltage
29	3.3V			3.3V Module Supply Voltage
30	3.3V			3.3V Module Supply Voltage
31	3.3V			3.3V Module Supply Voltage
32	3.3V			3.3V Module Supply Voltage
33	3.3V			3.3V Module Supply Voltage
34	3.3V			3.3V Module Supply Voltage
35	GND			Ground
36	MCLKn (VND_IO_B)	I/O		Monitor clock output for optical waveform testing or for recovered clock from optical input. Maybe used as Vendor I/O B.
37	MCLKp (VND_IO_C)	I/O		Monitor clock output for optical waveform testing or for recovered clock from optical input. Maybe used as Vendor I/O C.
38	GND			Ground

PIN #	NAME	I/O	Logic	Description
39	RX15n	O	CML	Received data output
40	RX15p	O	CML	Received data output
41	GND			Ground
42	RX13n	O	CML	Received data output
43	RX13p	O	CML	Received data output
44	GND			Ground
45	RX11n	O	CML	Received data output
46	RX11p	O	CML	Received data output
47	GND			Ground
48	RX9n	O	CML	Received data output
49	RX9p	O	CML	Received data output
50	GND			Ground
51	RX7n	O	CML	Received data output
52	RX7p	O	CML	Received data output
53	GND			Ground
54	RX5n	O	CML	Received data output
55	RX5p	O	CML	Received data output
56	GND			Ground
57	RX3n	O	CML	Received data output
58	RX3p	O	CML	Received data output
59	GND			Ground
60	RX1n	O	CML	Received data output
61	RX1p	O	CML	Received data output
62	GND			Ground

Figure 5-12 CFP8 Pin Map for Multiple Configurations

PIN #		400GAUI-16	200GAUI-8	CAUI-4	50GAUI-2	25GAUI			
BOT	TOP	x1	x2	x4	x8	x16			
1	124								
2	123	Ch. 0 TX Top & Bottom	Ch. 1 TX Top & Bottom	Ch. 3 TX Top & Bottom	Ch. 7 TX Top & Bottom	Ch. 15: Bottom			
3	122				Ch. 14: Top				
4	121								
5	120							Ch. 6 TX	
6	119						Top & Bottom		
7	118						Ch. 13: Bottom		
8	117						Ch. 12: Top		
9	116					Ch. 2 TX Top & Bottom	Ch. 5 TX Top & Bottom	Ch. 11: Bottom	
10	115							Ch. 10: Top	
11	114								
12	113							Ch. 4 TX Top & Bottom	Ch. 9: Bottom
13	112							Ch. 8: Top	
14	111								
15	110				Ch. 0 TX Top & Bottom	Ch. 1 TX Top & Bottom	Ch. 3 TX Top & Bottom	Ch. 7: Bottom	
16	109						Ch. 6: Top		
17	108						Ch. 2 TX Top & Bottom	Ch. 5: Bottom	
18	107							Ch. 4: Top	
19	106								
20	105			Ch. 0 TX Top & Bottom	Ch. 1 TX Top & Bottom	Ch. 3: Bottom			
21	104					Ch. 2: Top			
22	103								
23	102					Ch. 0 TX Top & Bottom	Ch. 1: Bottom		
24	101					Ch. 0: Top			
25	100								
26	99								
27	98								
28	97								
29	96								
30	95								
31	94								
32	93								
33	92								
34	91								
35	90								
36	89								
37	88								
38	87								
39	86	Ch. 0 RX Top & Bottom	Ch. 1 RX Top & Bottom	Ch. 3 RX Top & Bottom	Ch. 7 RX Top & Bottom	Ch. 15: Bottom			
40	85				Ch. 14: Top				
41	84								
42	83							Ch. 6 RX	
43	82						Top & Bottom		
44	81						Ch. 13: Bottom		
45	80						Ch. 12: Top		
46	79					Ch. 2 RX Top & Bottom	Ch. 5 RX Top & Bottom	Ch. 11: Bottom	
47	78							Ch. 10: Top	
48	77								
49	76							Ch. 4 RX Top & Bottom	Ch. 9: Bottom
50	75							Ch. 8: Top	
51	74								
52	73				Ch. 0 RX Top & Bottom	Ch. 1 RX Top & Bottom	Ch. 3 RX Top & Bottom	Ch. 7: Bottom	
53	72						Ch. 6: Top		
54	71						Ch. 2 RX Top & Bottom	Ch. 5: Bottom	
55	70							Ch. 4: Top	
56	69								
57	68			Ch. 0 RX Top & Bottom	Ch. 1 RX Top & Bottom	Ch. 3: Bottom			
58	67					Ch. 2: Top			
59	66								
60	65					Ch. 0 TX Top & Bottom	Ch. 1: Bottom		
61	64					Ch. 0: Top			
62	63								

5.9 CFP8 LABELING

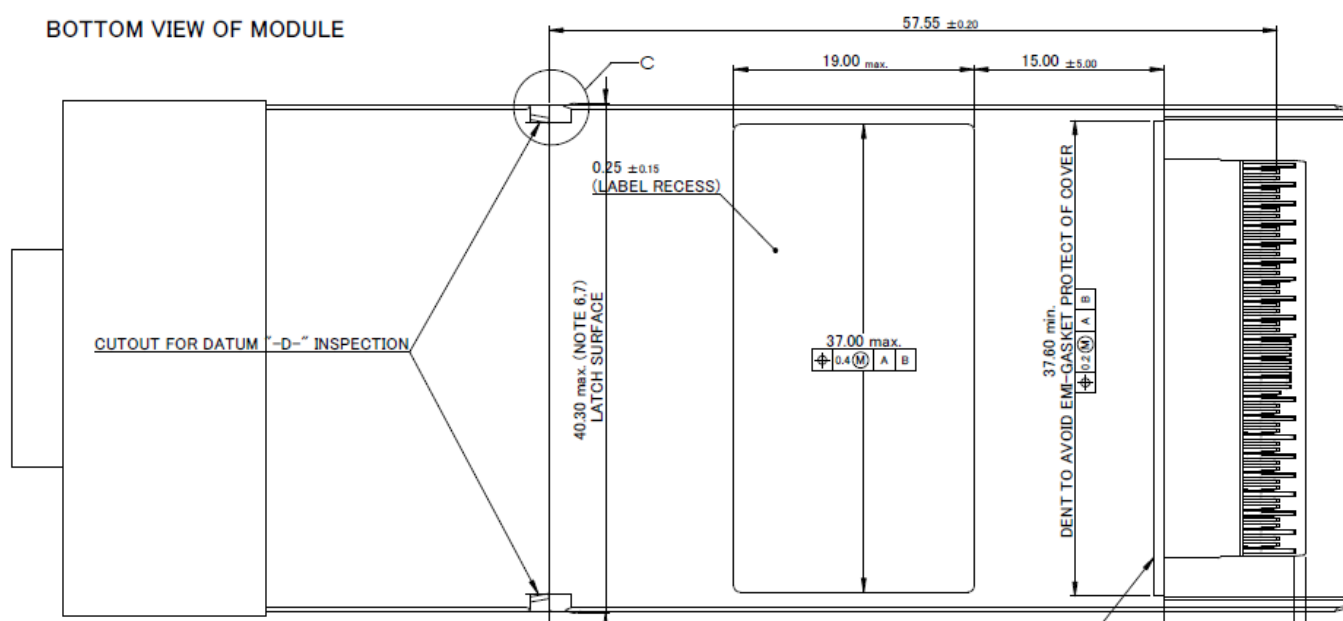
The CFP8 bail latch color is used to indicate the module optics application. The color codes are specified in Table 5-8.

Table 5-8: CFP8 Bail Latch Color Coding

Bail Latch Color	Minimum reach & Minimum loss
Beige	100m & 2dB (MMF)
Yellow	500m & 2.5dB (SMF)
Green	2km & 4dB (SMF)
Lighter Blue	10km & 6dB
Lighter Red	30km/40km
White	80km

The CFP8 module should be clearly labeled. The complete labeling need not be visible when the CFP8 module is installed in the host cage assembly. A recessed area on the bottom of the CFP8 module, as shown in Figure 5-13, is the recommended location for module label.

Figure 5-13: CFP8 Module Label Recess



6 REGULATORY COMPLIANCE

Per specifications given in Ref. [1].

-----End of Document-----